# Gas injection techniques for $Al_2O_3$ atomic layer deposition

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## Abstract

Metal-oxide-metal and metal-oxide-semiconductor capacitors are fabricating via atomic layer deposition (ALD) with $Al_2O_3$ as the dielectric. Different gas injection amounts and exposure times are used in order to determine the growth parameters that give optimal device characteristics. Oxide thickness, dielectric constant, C–V hysteresis, breakdown field, and leakage current are measured. While definite numerical trends were not observed for most of these characteristics, the measurements provided enough information to determine an optimal set of growth parameters.

## 1 Introduction

Aluminum oxide has attracted attention as a desirable dielectric for use in thin-film devices for its characteristics that outshine those of silicon oxide, the traditional dielectric used in thin-film devices. $SiO_2$, at small thicknesses, is susceptible to high leakage currents due to quantum tunneling as well as surface irregularity.[1] $Al_2O_3$, on the other hand, has excellent surface uniformity as well as stoichiometric uniformity, and a dielectric constant that is nearly twice that of silicon dioxide.[2,3]

$Al_2O_3$ has been deposited with astounding efficacy using the technique of atomic layer deposition (ALD). Atomic layer deposition creates $Al_2O_3$ one monolayer at a time, allowing the user to precisely control the thickness of the oxide.[4] Additionally, atomic layer deposition can be performed at temperatures of 100-300°C, which is much cooler than the conditions necessary for $SiO_2$ growth, a thermal process that occurs at around 1000°C.[5]

One monolayer of $Al_2O_3$ is grown in two steps. First, trimethylaluminum (TMA) gas is injected into the chamber and yields the following reaction:

$$Al - OH + Al(CH_3)_3 \rightarrow Al - O - Al(CH_3)_2 + CH_4$$

Next, water vapor is injected into the chamber, and then the second step of the reaction occurs:

$$Al - CH + H_2O \rightarrow Al - OH + CH_4$$

[6] This is the reaction that aggregates a layer of $Al_2O_3$ onto a previous layer of $Al_2O_3$— however, the $Al_2O_3$ is always initially deposited onto a substrate that is

[1] Groner, M.D. Electrical characterization of thin $Al_2O_3$ films grown by atomic layer deposition on silicon and various metal substrates. Accessed via Elsevier database. 10 Apr 2006. http://www.elsevier.com

[2] Ibid.

[3] Biercuk, M.J. Low-temperature atomic-layer-deposition lift-off method for microelectronic and nanoelectronic applications. Accessed via American Institute of Physics database. 10 Apr 2006. http://apl.aip.org/

[4] See 1.

[5] Groner, M.D. Low-Temperature Al2O3 Atomic Layer Deposition. Accessed via American Chemical Society. 20 Apr 2006. http://pubs.acs.org/

[6] Ibid.

not $Al_2O_3$, but more likely Si, another semiconductor, or a metal. Assuming that $Al_2O_3$ has identical nucleation behavior on Si as it does on $Al_2O_3$, the first stage of the reaction would look like this:

$$Si - H \rightarrow Si - O - Al(CH_3)_2$$

but in fact, on Si(1 0 0), it has been shown[7] that the reaction occurs more accurately as thus:

$$Si - H \rightarrow Si - O - Al(CH_3)_2 + Si - CH_3$$

Notice the $Si - CH_3$ group— this group is unable to participate in the second stage of the reaction, and in essence forms a dead end in the nucleation of the $Al_2O_3$. The focus of this research is to minimize the occurence of this "dead end" group and achieve optimal $Al_2O_3$ growth by changing the growth parameters of the first few cycles, and to observe the effect on an $Al_2O_3$ device's characteristics by changing said parameters. In this experiment, two different types of devices will be fabricated with a total of 12 different $Al_2O_3$ oxides grown via ALD, and their device characteristics will be evaluated in hopes of determining an optimal set of $Al_2O_3$ oxide growth parameters.

# 2 I–V Device Fabrication

Metal-oxide-metal capacitors were fabricated to generate I–V curves, and from these curves critical device parameters can be determined, such as the amount of electric field necessary to cause catastrophic breakdown of the oxide dielectric (known as breakdown field strength) and the amount of leakage current through a capacitor undergoing a voltage bias. Two varities of I–V devices were created: one that measures 100 $\mu$s on a side (yielding an area of $1 \times 10^{-4}$cm$^2$) and one that measures 300 $\mu$m on a side (yielding an area of $9 \times 10^{-4}$cm$^2$).

## 2.1 Metal Evaporation

First, a layer of chromium metal is evaporated on an Si(1 0 0) wafer. The silicon does not play any role in the I–V device besides to act as a surface upon which to fabricate the I–V devices, and therefore does not need to be cleaned of oxide or any other materials. The chromium was evaporated using the Denton DV-502A Electron Beam Evaporator, which evaporates chromium at pressures of $2 \times 10^{-6}$ Torr. A chromium layer with a thickness of 1000Å was deposited on the Si wafer at a rate of 2–6 Å/s.

## 2.2 Photolithography & Cr Etch

Next, the chromium is patterned and etched using photolithography. After the wafer has been prebaked at 120°C on a hot plate for five minutes, a layer of hexamethyldisilazane (HMDS) is spun on to the wafer for 40 sec at a speed of 4000 rpm/s, and then a layer of AZ5214 photoresist is spun on to the wafer for the same duration and at the same speed. After a soft bake for one minute at 95°C on a hot plate, the photoresist is ready for UV exposure. The photolithography mask, which was created with the Heidelberg DWL66 Laser Writer, is aligned to the wafer with the Karl Suss MA6 Mask Aligner. Using a soft contact between the sample and the mask, the photoresist was exposed to 2.0 W 365 nm UV light for 40 sec with a 40 $\mu$m Al gap. The photoresist is then developed with a 1:1 312MF:$H_2O$ solution for about 30 sec, then is hard baked at 95°C for 5 min.

The chromium is then etched with CR-7 for approximately 90 sec. Once the chromium is fully etched, the photoresist is stripped by placing the wafer in a bath of Baker's PRS1000 at 100°C, which is itself placed in an ultrasound bath for 1 min to ensure complete removal of the photoresist.

The end result of the metal evaporation, photolithography, and Cr etch is the creation of the bottom contact for the capacitor.

## 2.3 Atomic Layer Deposition of $Al_2O_3$

Now that the bottom contact has been created, the oxide can be grown. The oxide is grown via ALD with the Cambridge NanoTech Savannah 100.

The Savannah 100 is able to be programmed with several different growth parameters including growth temperature, gas pulse time, gas exposure time, gas

[7] Frank, Martin M. Nucleation and interface formation mechanisms in atomic layer deposition of gate oxides. Applied Physics Letters Vol. 26 Num. 26 30 Jun 2003. Accessed via Google Scholar. http://scholar.google.com

pumping time, and inert gas flow rate. For all growth combinations in this study, the growth temperature was kept constant at 250°C, and the inert gas ($N_2$) flow rate was kept constant at 20 sccm.

Twelve different growth combinations were evaluated, with two different steps in the growth being altered: the pretreatment phase and the growth phase.

#### 2.3.1 Pretreatment Phase

Three different pretreatments were performed on the samples. Each pretreatment consists of five cycles. The concept behind the selection of parameters for these three pretreatments was that the exposure time should be increased approximately one order of magnitude on each sample.

The only parameters that differ between the pretreatment phase and the growth phase change are the exposure and pumping times. The amount of reactive gas introduced into the chamber during the pretreatment phase (known as "pulse time") is identical to the pulse time for the actual growth phase.

Also, note that Pretreatment 0 is named such because its parameters are identical to the growth phase parameters, so it is as if a pretreatment was never performed on the sample.

| Name | Exposure (s) | Pump (s) |
|---|---|---|
| Pre 0 | 0 | 5 |
| Pre 1 | 25 | 25 |
| Pre 2 | 240 | 25 |

#### 2.3.2 Growth Phase

After the pretreatment is performed, then the remainder of the oxide is grown. The sample is then exposed to 495 cycles at normal growth rates. Because Cambridge NanoTech's recommended gas pulse time was between 0.07 sec and 0.1 sec, values were chosen that are significantly over and under these recommended times for the sake of completeness.

For all growth phases, the gas exposure time was 0 sec, and the gas pump time was 5 sec. Note that while the "gas exposure time" was 0 sec, this does not mean that the sample was exposed to the gas for exactly 0 sec— it takes approximately 2 seconds for the pump to evacuate all of the reactive gas in the chamber.

| Name | Pulse (s) |
|---|---|
| Gas 1 | 0.015 |
| Gas 2 | 0.06 |
| Gas 3 | 0.1 |
| Gas 4 | 0.2 |

The result of the pretreatment and growth phases is the exposure of the sample to exactly 500 cycles of TMA and $H_20$, which should ideally yield 550 Å of oxide.

### 2.4 Top Contact Fabrication

Once the oxide is grown, then the top contact of the capacitor can be created. The steps of metal evaporation, photolithography, and chromium etch are simply repeated, the only difference being the orientation of the photolithography mask is rotated 180° to create a symmetrical device where both the top and bottom contacts are visible.

### 2.5 Photolithography & Oxide Etch

The final step is to cut a hole in the $Al_2O_3$ layer in order to expose the bottom contact of the capacitor. This is accomplished by repeating the application of photoresist and UV exposure via photolithography, only a different mask is used. Once the photoresist is developed, the wafer is exposed to 10:1 DI $H_2O$:HF for approximately 90 sec to etch the oxide. The photoresist is then stripped using the aforementioned PRS1000 technique, and the device is ready for testing.

## 3 C–V Device Fabrication

Metal-oxide-semiconductor (MOS) devices were fabricated to obtain a characteristic C–V plot, from which the dielectric constant and hysteresis shift of said devices can be determined.

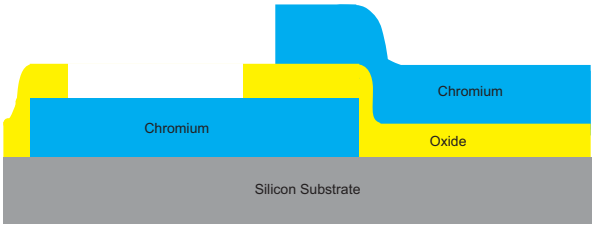



Figure 1: The layers of the I–V device.

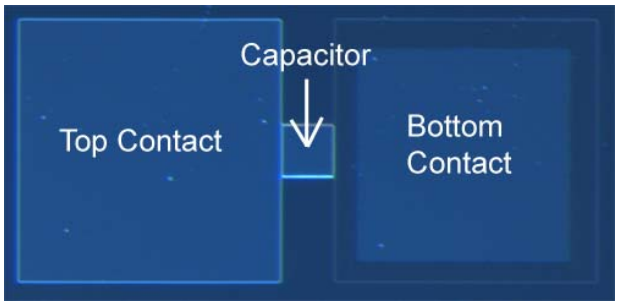



Figure 2: The 100 $\mu$m I–V device.

### 3.1 Wafer Clean

Since the Si(1 0 0) is one of the contacts of the MOS capacitor, there must be no foreign material between it and the $Al_2O_3$ that is to be grown upon it, including any $SiO_2$ that may accumulated simply by the Si wafer being exposed to air. In order to remove any aggregated foreign matter from the wafer we subject it to the following chemical treatment:

1. 1:1:5 $NH_4OH : H_2O_2 : H_2O$ at 80°C for 15 min (removes organic matter)
2. $H_2O$ rinse 5 min
3. 1:10 $HF : H_2O$ at room temperature for 1 min (removes oxide)
4. $H_2O$ rinse 5 min
5. 1:1:5 $HCl : H_2O_2 : H_2O$ at 80°C for 15 min (removes metal ions)
6. $H_2O$ rinse 5 min

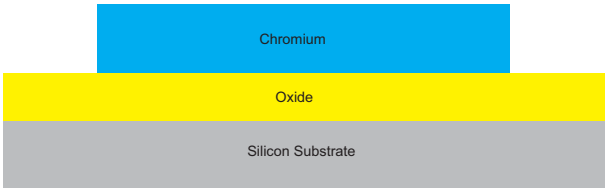



Figure 3: The layers of the C–V device.

### 3.2 Atomic Layer Deposition of $Al_2O_3$

The varying parameters used to grow the oxide on the I–V devices are identical to those used to grow the C–V devices. The I–V and C–V devices of each corresponding gas and pretreatment variety were grown simultaneously in the same chamber, and so should have identical properties.

### 3.3 Top Contact Fabrication

All that remains to fabricate the C–V device is to create a chromium contact on top of the oxide. These contacts were fabricated in an identical fashion as the top side contacts on the I–V devices, except a different mask was used that contained an array of simpler squares of different size. The first four samples have square contacts that are 500 $\mu$m, 750 $\mu$m, and 1000 $\mu$m in length on one side, while the later eight samples have square contacts that are 500 $\mu$m, 400 $\mu$m, and 300 $\mu$m in length on one side for reasons that will be discussed later.

## 4 Measurements

After device fabrication was completed, the devices were then tested for the following characteristics: oxide thickness, breakdown field, leakage current, dielectric constant, C–V hysteresis.

It should be noted that the Gas 4 Pretreatment 0 performed extraordinarily poorly in the tests. This is mostly likely due to the fact that directly after oxide growth, both the C–V and the I–V sample appeared to have an unexpected speckling of white in the normally uniformly brown oxide. This may have been

due to an anomalous malfunction in the ALD machine. Unfortunately, there was not enough time to fabricate another Gas 4 Pretreatment 0 sample, so all measurements for the Gas 4 Pretreatment 0 will be incongruous with the rest of the data, or will be omitted altogether.

## 4.1 Oxide Thickness

The thickness of each sample's oxide was measured using the Gaertner L3W16 Ellipsometer. The measurements were taken on the C–V sample directly following the growth of the oxide (i.e. before the chromium was deposited). The C–V samples were used because the index of refraction of their clean Si substrate was entirely predictable, whereas the I–V samples were not cleaned and therefore could possess some surface oxides or other impurities that would distort the ellipsometer's readings.

| Name | Thickness (Å) |
|---|---|
| Gas 1 Pre 0 | 460.1 |
| Gas 1 Pre 1 | 468.0 |
| Gas 1 Pre 2 | 468.5 |
| Gas 2 Pre 0 | 492.7 |
| Gas 2 Pre 1 | 501.4 |
| Gas 2 Pre 2 | 499.3 |
| Gas 3 Pre 0 | 522.6 |
| Gas 3 Pre 1 | 536.6 |
| Gas 3 Pre 2 | 518.0 |
| Gas 4 Pre 0 | 528.7 |
| Gas 4 Pre 1 | 545.5 |
| Gas 4 Pre 2 | 551.8 |

From the table, we can discern two trends in the oxide thickness according to the gas and pretreatment types:

1. As the amount of reactive gas injected into the chamber increases, so does the oxide thickness.

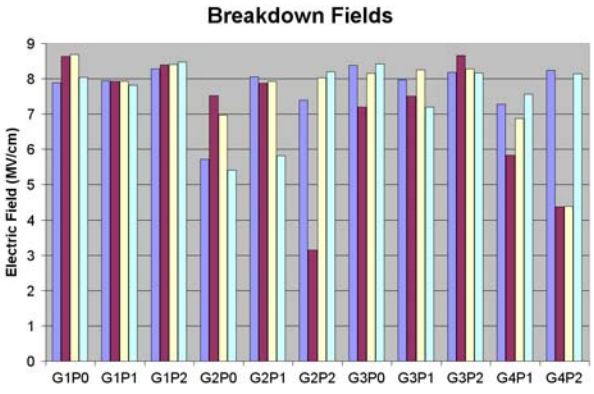
2. For any given amount of reactive gas injection, a surface that is pretreated (either Pretreatment 1 or Pretreatment 2) will result in a thicker oxide than one that is not pretreated (Pretreatment 0).

Whether Pretreatment 1 or Pretreatment 2 yields a thicker oxide is not easily determined— for Gas 1, Pretreatement 2 is nearly identical to Pretreatment 1, for Gas 2 and Gas 3, Pretreatment 2 is significantly thinner than Pretreatment 1, and for Gas 4, Pretreatment 2 is significantly thicker than Pretreatment 1.

## 4.2 Breakdown Field Strength

The breakdown electric field strength of the oxide was tested on the I–V devices with Keithley Model 2400 Voltage/Current measurement stack. A bias was swept from 0 to 50 Volts across the 100 $\mu$m devices until they catastrophicaly broke down, and the voltage at which they did this was recorded. Four devices were tested on each sample.

From the graph it is visible that every variety of oxide has a breakdown electric field strength of around 8 MV/cm, with a number of devices failing before this point, most likely due to point defects in the oxide of that particular device that facilitate the breakdown of the oxide. Because only four samples were taken, it is unable to be determined whether or not any particular sample has a statistically relevant inclination or disinclination to have these faulty devices.




## 4.3 Leakage Current

The leakage current through I–V devices under a 5 V bias was measured with the HP4145B Semiconductor

Parameter Analyzer. Four different 300 $\mu$m devices were tested on each sample.

The graph of these leakage current shows similar behavior to the breakdown field strengths. There is a general trend of devices having a leakage current of 1–5 pA with some devices showing characteristics of defects— however, unlike the breakdown field strengths, in which defective devices were identified by breaking down 2–3 MV/cm sooner, the leakage currents in defective devices vary up to seven orders of magnitude.

These tremendously high currents are most likely caused by pinhole defects in the oxide, where the chromium has evaporated into the crevace enough to conduct directly to the opposite plate, or to be close enough to the other plate to the point where electron tunneling creates significant current through the oxide.

The only curious anomalies exist with the Gas 1 Pretreatment 0, Gas 4 Pretreatment 1 and Gas 4 Pretreatment 2 samples, which showed consistent leakage currents of 50–100 pA. Since there are no obvious similarities between these devices, it is possible that these anomalies are due to some artifact of the fabrication process and are not correlated to the properties of the oxide.

I should note here that Gas 1 and Gas 2 type samples were very prone to melting when a bias voltage in excess of 8V or so was applied to them. This is most likely due to high temperatures generated by the very high currents that can occur when chromium contact or tunnelling occurs across the oxide. Not only would these devices melt between the capacitor plates, but they would also melt over the contact pads, which begs the possibility of electrons traveling through the oxide to the silicon substrate, conducting through the silicon and out of the sample, or sometimes even traveling upwards through the oxide again and into the other chromium pad. The Gas 3 and Gas 4 devices were markedly more resistant to this bizarre type of failure, and would therefore be more advisable for use in high-voltage applications.

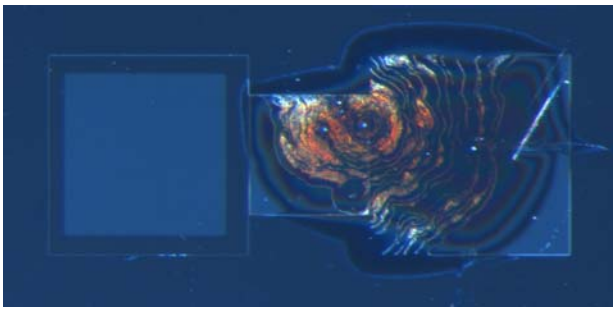
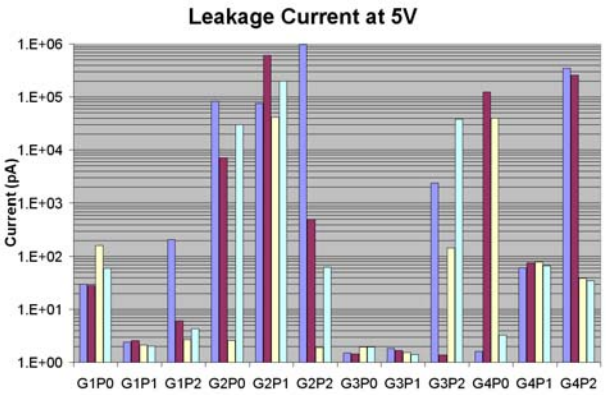


Figure 4: A melted 300 $\mu$m Gas 1 device.




## 4.4 Dielectric Constant

The dielectric constant of the various samples was obtained by evaluating their C–V plots. For the C–V plots, a bias voltage was swept from $-5$ V to 5 V over the C–V devices as the capacitance was measured using the Micromanipulator Model 410 C–V Plotter.

The dielectric constant of a capacitor can be obtained with the following equation:

$$\varepsilon_{Al_2O_3} = \frac{C_{acc} \cdot t_{ox}}{A \cdot \varepsilon_0}$$

where $\varepsilon_{Al_2O_3}$ is the dielectric constant, $C_{acc}$ is the accumulation capacitance, $t_{ox}$ is the oxide thickness, A is the area of the capacitor, and $\varepsilon_0$ is the permittivity of free space.

While four of the samples have capacitor sizes of 500, 750, and 1000 $\mu$m, the accumulation capaci-

tances of these devices did not scale with the area of the capacitors as they should. It was clear that some other mechanism was reducing the efficacy of these large devices, so a new array of capacitors with sizes of 500, 400, and 300 $\mu$m was implemented, and these devices scaled much better. For the sake of consistency, all C–V measurements were done with the 500 $\mu$m devices.

| Name | $\varepsilon_0$ |
|---|---|
| Gas 1 Pre 0 | 5.4 |
| Gas 1 Pre 1 | 5.9 |
| Gas 1 Pre 2 | 7.0 |
| Gas 2 Pre 0 | 7.0 |
| Gas 2 Pre 1 | 5.7 |
| Gas 2 Pre 2 | 7.2 |
| Gas 3 Pre 0 | 6.4 |
| Gas 3 Pre 1 | 6.8 |
| Gas 3 Pre 2 | 7.1 |
| Gas 4 Pre 1 | 6.9 |
| Gas 4 Pre 2 | 7.5 |

The data shows a measured dielectric constant for almost all samples that hovers around the value of 7.0, except for the Gas 1 Pretreatment 0, Gas 1 Pretreatment 1, and Gas 2 Pretreatment 1 samples, which are around 5.6. This may be correlated to the lower amounts of gas are used in these samples, or it may be just be random occurence— after all, if it were correlated to the lower gas levels, then one would expect the Gas 1 Pretreatment 2 and Gas 2 Pretreatment 0 samples to have significantly lower dielectric constants.

### 4.5 Hysteresis

The amount of hysteresis in the C–V curve was also measured. It was proposed that the $Si - CH_3$ groups that arise during oxide nucleation may be creating "holes" where non-native charges could become trapped; oxides with more of these holes would exhibit more hysteresis since charges would build up in the oxide when the capacitor goes into the accumulation regime. Like the measurement of the dielectric constant, the voltage was swept across a C–V device from $-5$ V to 5 V, but this time it was swept back down to $-5$ V as well.

| Name | Hysteresis Shift (V) |
|---|---|
| Gas 1 Pre 0 | 0.75 |
| Gas 1 Pre 1 | 0.51 |
| Gas 1 Pre 2 | 0.88 |
| Gas 2 Pre 0 | 0.30 |
| Gas 2 Pre 1 | 0.85 |
| Gas 2 Pre 2 | 0.33 |
| Gas 3 Pre 0 | 0.51 |
| Gas 3 Pre 1 | 0.63 |
| Gas 3 Pre 2 | 0.65 |
| Gas 4 Pre 1 | 0.30 |
| Gas 4 Pre 2 | 0.48 |

From the table of data, there appears to be no correlation between the amount of hysteresis and the growth parameters of the oxide. The standard deviation of these numbers is only 0.2 V, so it is very possible that the fluctuations in the amount of hysteresis shift are totally spontaneous.

## 5 Conclusions

As we have seen, the only device characteristic that quantifiably varies from sample to sample is the thickness of the oxide grown. All other characteristics have rather fuzzy relationships with the growth parameters. Nonetheless, it is possible to get a concrete idea of what the ideal parameters may be.

First of all, the more gas that is used, the more the thickness of the oxide approaches the ideal value, which is 1.1 Å/cycle. If we want to be able to grow oxides to a specific thickness, then using more gas is advisable.

Secondly, if we want to protect against our devices melting under moderate voltages, then we should definitely avoid Gas 1 devices and probably Gas 2 devices. These had a very high occurence of structural failure and would not be appropriate where any sort of device reliability is desired.

Third, high gas devices (Gas 3 and Gas 4) were more likely to have normal dielectric constants (around 7.0) where low gas devices (Gas 1 and Gas

2) tended to have more abnormal oxides with lower dielectric constansts.

Fourth, Gas 4 devices often displayed puzzling characteristics, such as the consistantly abnormally high leakage currents in the Gas 4 Pretreatment 1 and Gas 4 Pretreatment 2 devices, and the total defectiveness of the Gas 4 Pretreatment 0 devices. It is likely that the large amount (compared to to the manufacturer's recommendation) of reactive gas injected into the chamber produces temperamental and unpredictable devices. Furthermore, exceptionally large amounts of reactive gas have the propensity to react and form crystals in the air rather than on the wafer, which in turn get pumped out of the chamber and eventually erode the pumping mechanism in the ALD machine.

Fifth, the marked difference in oxide thickness between Pretreatment 1 & 2 and Pretreatment 0 devices show that it is worthwhile to bother with doing pretreatments— however, there is no evidence across the board to suggest that there is any difference in device characteristics engendered by using Pretreatment 2 rather than Pretreatment 1. It logically follows, then, to use the Pretreatment 1 technique, because the process runs ten times as quickly.

Considering these five points, it makes most sense to use the growth parameters of a Gas 3 Pretreatment 1 device to achieve the most reliable and desirable device characteristics. For each measurement test the Gas 3 Pretreatment 1 device had desirable device characteristics: near-ideal oxide thickness, low and consistent leakage current, high and consistent breakdown field, near-ideal dielectric constant, and a permissible amount of C–V hysteresis.

# 6 Acknowledgements

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