Tile Current Monitor Peer Review

Work Planning Number (LLD # 1382)

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Thanks to: H. Kugel, H. Takahashi, R. Ellis, J. Lawson

- Basic Requirements
- Mechanical Design (Show and Tell)
- Resistive Element Specification
- Thermal Considerations
- Electronics
- Feedthroughs And Field Cables
- Calibration
- Summary

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Goal: Measure Currents Flowing into the OBD

- Halo Currents
  - If vertical position control is lost and plasma comes in contact with the vessel, currents link the plasma and PFCs.
  - These currents can cause destructive JxB forces, so important in understand their origin and scaling.
  - LLD is designed to handle these currents.
  - Improved understanding will help in the design of LLD-2
  - *This is my (SPG) primary motivation for the present system.*

- SOL Currents
  - Smaller currents are known to flow into (or out of) DIII-D tiles during the I_p flat-top.
  - These have been implicated as playing a role in ELM and pedestal physics (Takahashi, Zakharov).
  - The proposed system has the capacity to begin to study this.
  - This is EF's primary source of interest.

- CHI Currents
  - OBD is one electrode for CHI.
  - If CHI currents pass through these tiles, then we can use them for injector current uniformity studies.

All of these topics could benefit from an upgrade in coverage beyond this initial proposal.

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Basic Features of the Design

Resistive Shunt

- Resistor element made from folded stainless shim-stock.
- Layers are insulated from each other with mica sheet.
- Stainless wires (0.015”) welded into the folds.
- Total Height: 0.07” (half-height: 0.035”)

Tile Isolation

- T-bar bolts are ceramic (sapphire) coated on their heads, as are washers.
  - Coating sample being testing right now, alumina coating technique as a backup.
- Additionally, use mica washers to insulate the washers.
- Oversized Mica sheets isolate tile corners from OBD.
- Result, T-bar is at tile potential, bolts are at OBD potential.

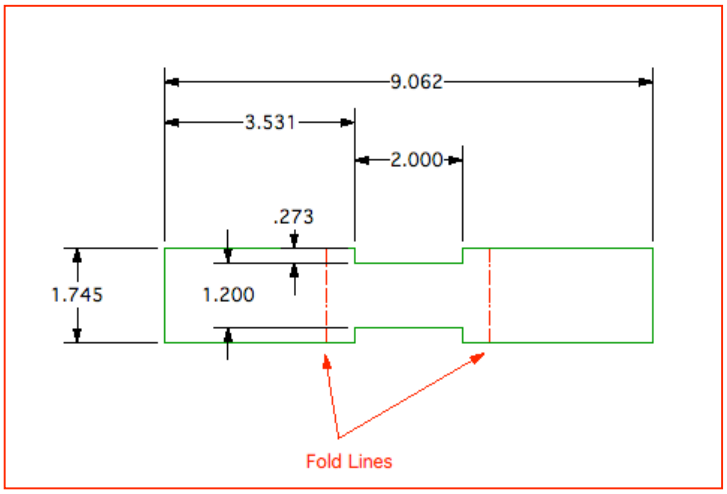
Tile and T-bar Modifications

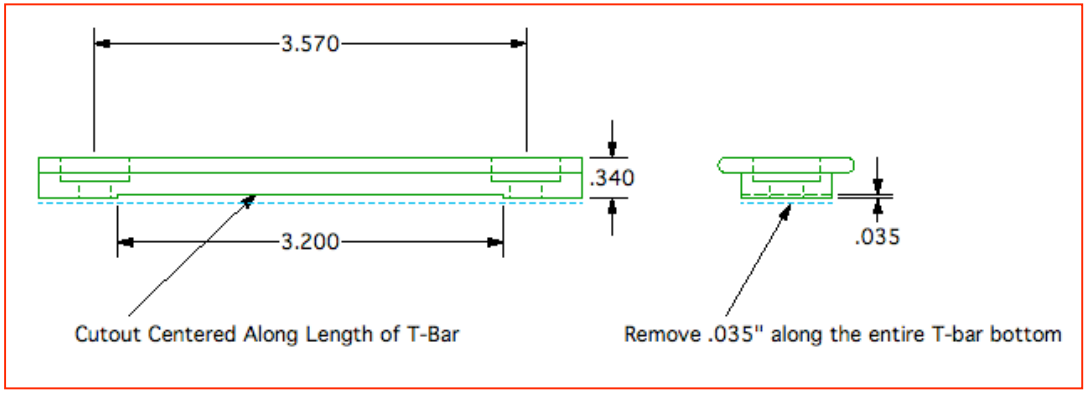
- Machine 0.035” off of entire tile bottom
- Machine a shallow (.035” deep) pocket in the tile bottom hold the sensor.
- Machine .07 from bottom of T-bar in region of pocket.

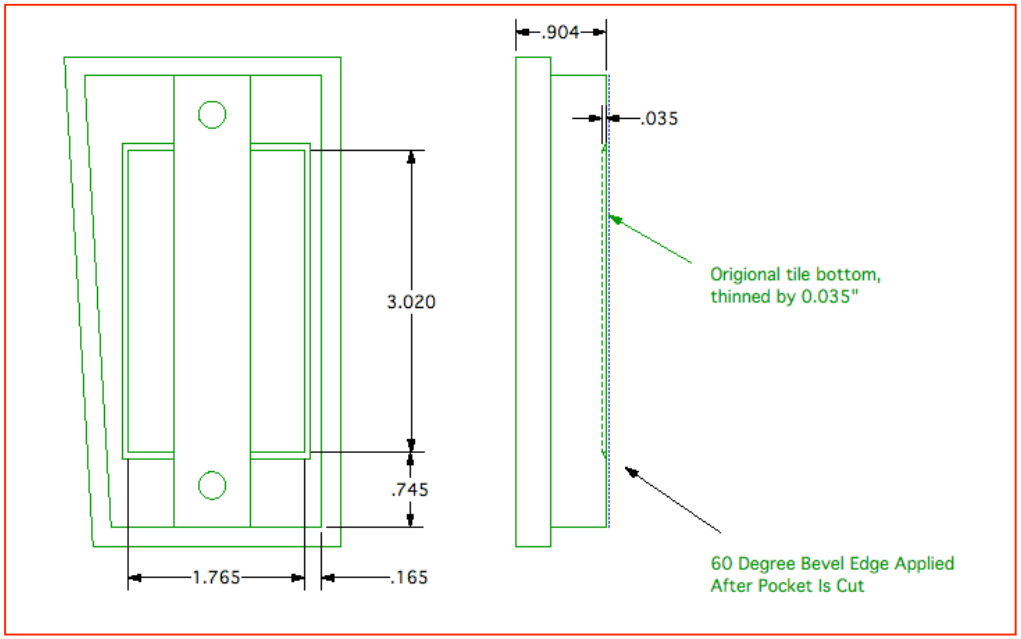
Modifications to OBD

- None

Preliminary Drawings For Modifications Are Finished







To Do

- Finalize drawings for T-bar and tile modifications
- Do those modifications
- Finish fabrication of shunts
- Assemble the final product.

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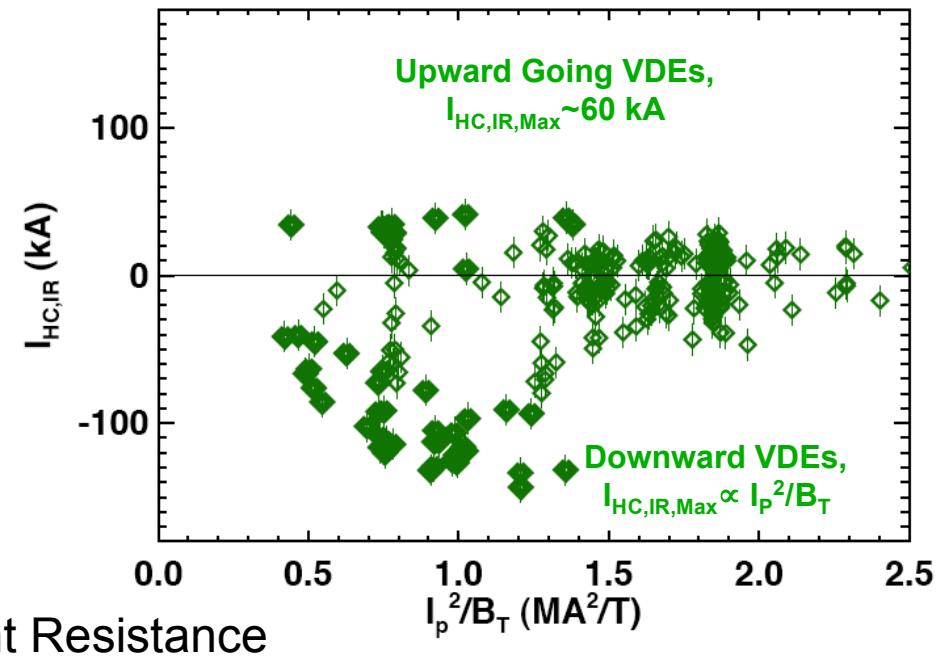
What currents to design for?

What We Know

- Measurements of net Halo current into OBD top out at ~150kA (triggered VDE), with ~40 kA fairly common (RWMs, locked islands).
- Spatial distribution in OBD is not resolved (this is the reason for this measurement).

Inner Ring, I_{HC} vs $I_P^2/B_T \sim I_P/q$



Constants For a Calculation of the Shunt Resistance

- A_{tile}: the area of a tile, .007 m^2
- τ: duration of halo current pulse, assumed triangular
- J_{HC}: the Halo current density, 260 kA/m^2 during disruptions, and 2.6kA/m^2 for equilibrium SOL currents.
  - 150 kA into OBD, into a 10cm Halo region at R=0.9 m
- $s_{inconel}$: specific heat of SS, 500 J/(kg K)
- $\rho_{inconel}$: Mass density of SS, $8.x10^3$ kg/m^3
- $\eta_{inconel}$: resistivity of SS $0.72x10^{-6}$ ohm m

Voltage and Temperature Requirements Determine the Shunt Parameters

l = length of resistive element, w = width of resistive element,
d = depth (thickness) of resistive element

Resistance of Shunt $$R_{sensor} = \frac{l\eta}{wd}$$

Voltage on Shunt $$V_{sensor} = \frac{l\eta}{wd} J_{HC} A_{tile}$$

Power Into Shunt $$P = J_{HC}^2 A_{tile}^2 \frac{l\eta}{wd}$$

Temperature Rise of Shunt $$\delta T = \frac{\tau}{2} J_{HC}^2 A_{tile}^2 \frac{\eta}{w^2 d^2 \rho s}$$

J (kA/m^2)	A_{tile} (m^2)	I (A)	τ (sec)	l (m)	w (m)	d (m)	V_{sensor} (V)	δT (C)
265	.007	1970	.005	.05	.03	.00025	9.4	31
2.65	.007		2	.05	.03	.00025	.1	1.2

Resistor (5mΩ) can tolerate both disruption transients and long-time SOL currents. Wide dynamic range requires dual-output electronics.

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Tile Heating (1)
Assessment Method

Estimate Temperature Rise

- Tile Volume: 188 cm^3
- Graphite Volumetric Heat Capacity, C:1.53 J cm^{-3} K^{-1}
- Fraction of total power to tile: .1/(2*3.14*1.3)=12x10^{-3}
- Total energy to tile: 1.3*6,000,000*12x10^{-3}= 93kJ
- Temperature Rise: 322 K

Estimate Temperature Decay

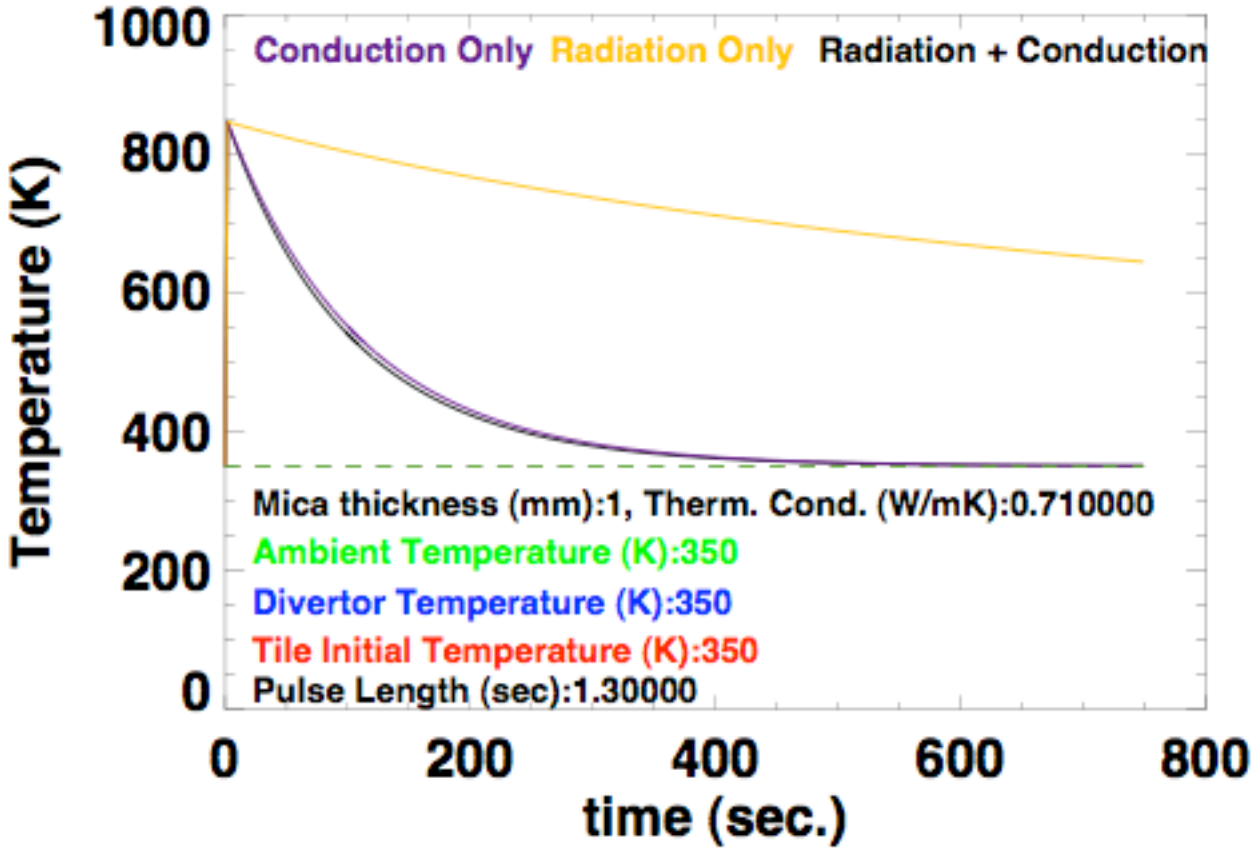
$$V_{tile} C_G \frac{dT}{dt} = -\frac{k_{mica} A_{mica} \left(T - T_{div}\right)}{t_{mica}} - eA_{side}\sigma\left(T^4 - T_{div}^4\right) - eA_{top}\sigma\left(T^4 - T_{Ves}^4\right)$$

t_{mica}=mica thickness (.001 m)
k_{mica}=mica thermal conductivity (0.7 W/mK)
T_{div}=temperature of lower divertor.
T_{div}=temperature elsewhere in the vessel
A_{side}=Area of tile radiating toward adjacent tiles
A_{top}=Area of time radiating toward top of machine.
σ=5.67e-8 W/m^2K^4
e=emissivity (0.3)
V_{tile}=Volume of tile

Solve this Equation Numerically!

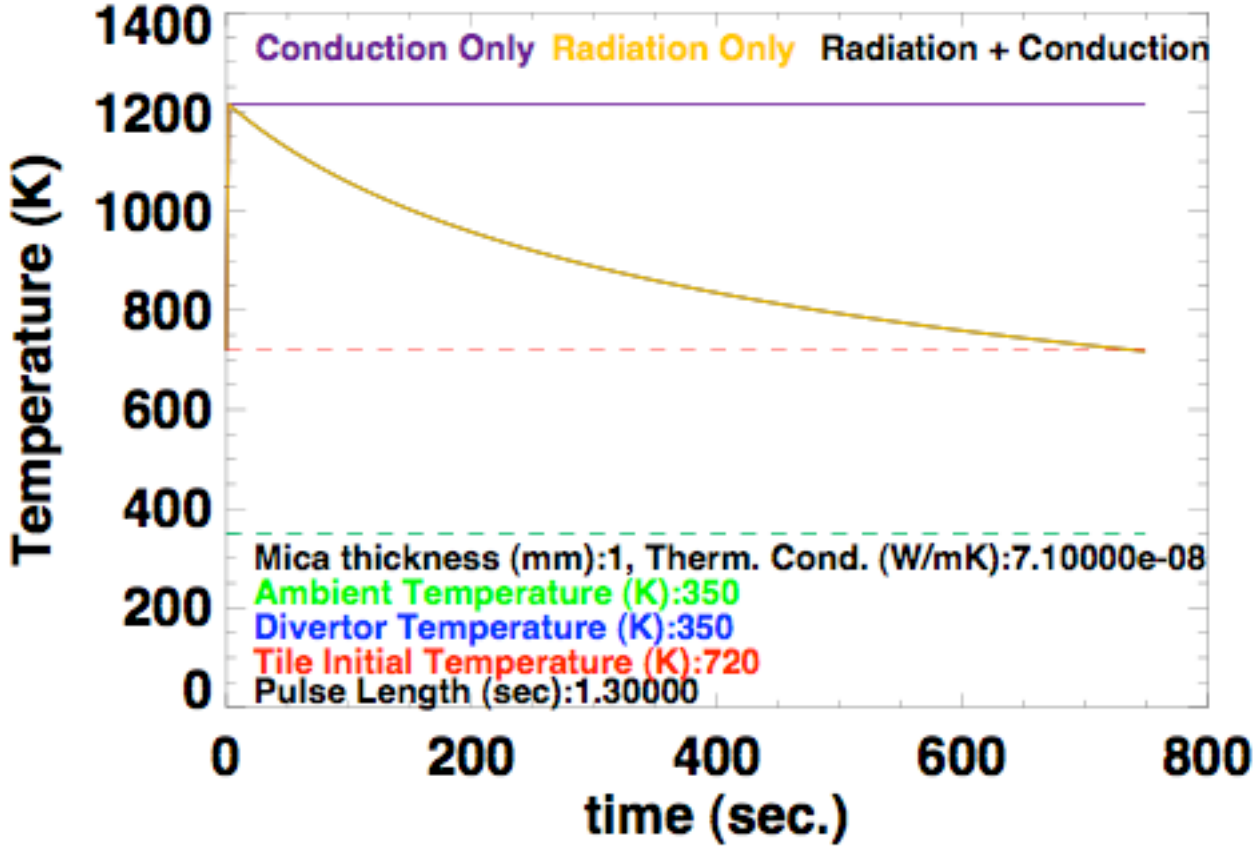
http://www.engineeringtoolbox.com/emissivity-coefficients-d_447.html
Stainless Steel, weathered, 0.85
Stainless Steel, polished, 0.075
Asphalt, 0.93
Black Enamel Paint, 0.80

Tile Heating (2)
Taking Full Credit For Conduction Through Tile Bottom



But, given layered design, can I take full credit for conduction?

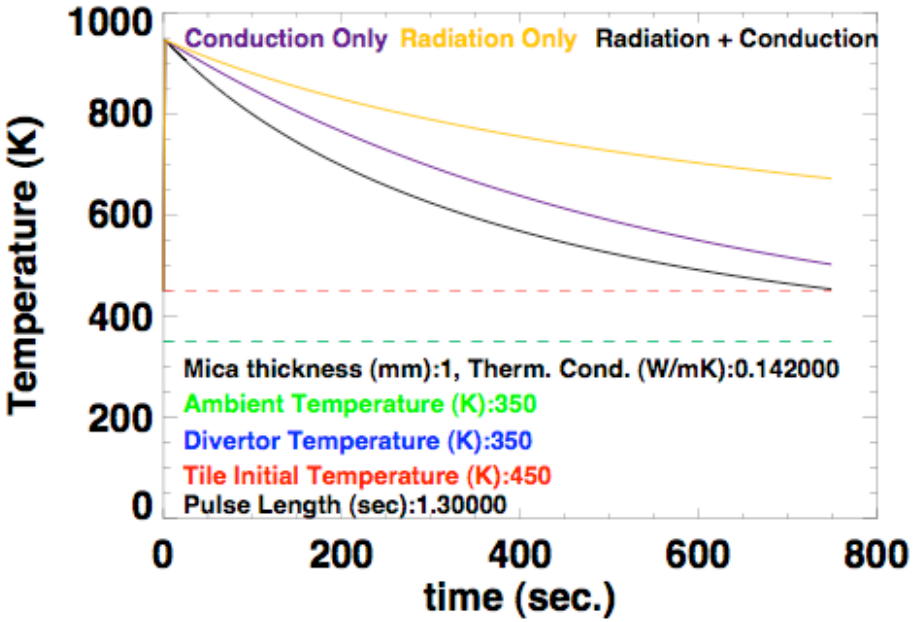
Tile Heating (3)
Assume No Conduction, Only Radiation



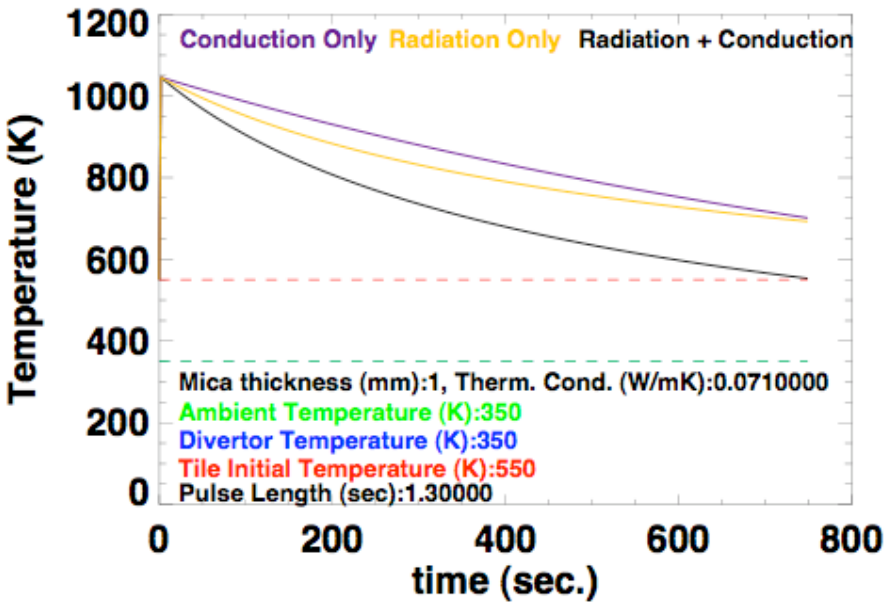
After Ratcheting Has Equilibrated, pre-shot temperature is 720K=446 C=836 F
Very Pessimistic: e=0.3, SOL completely covering tile, no conduction.

Tile Heating (4)
Try Two Intermediate Cases

Conduction is 5 Times Smaller
Ratchets to 450 K = 176 C



Conduction is 10 Times Smaller
Ratchets to 550 K=276C



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Requirements For BOTH HC and SOLC sensitivity

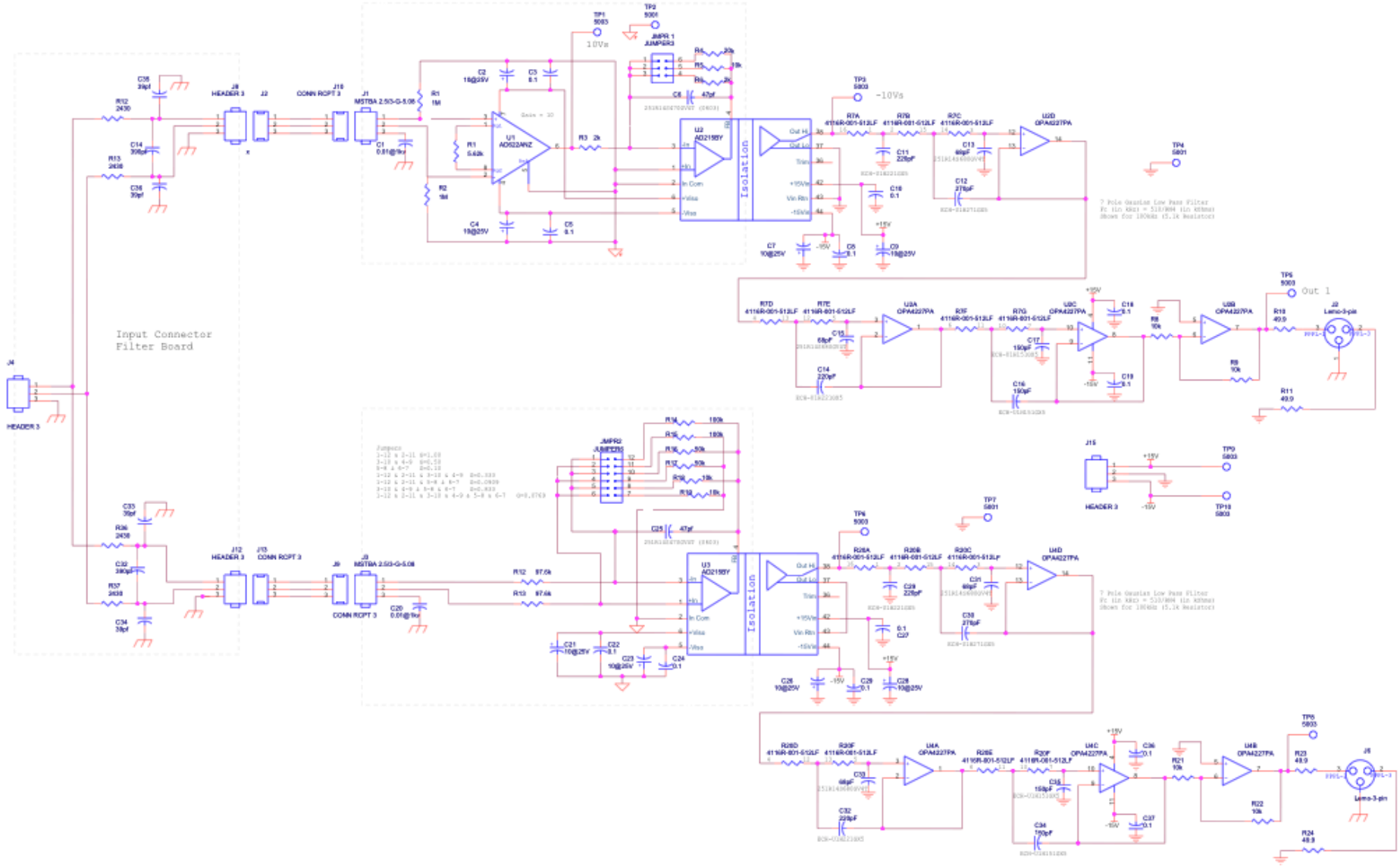
Requirements

- Requested 100kHz max. bandwidth, with capability to reduce for slower digitizer.
- Would like two outputs:
  - High gain for SOLCs (G=100 gives 0.5V for 1A into tile)
  - Low gain of HCs. (G=0.5 gives 5V for largest assumed HC)
- Need DC isolation
  - Need to break ground loops
  - Rack potential can deviate from outer vessel by ~100-200V

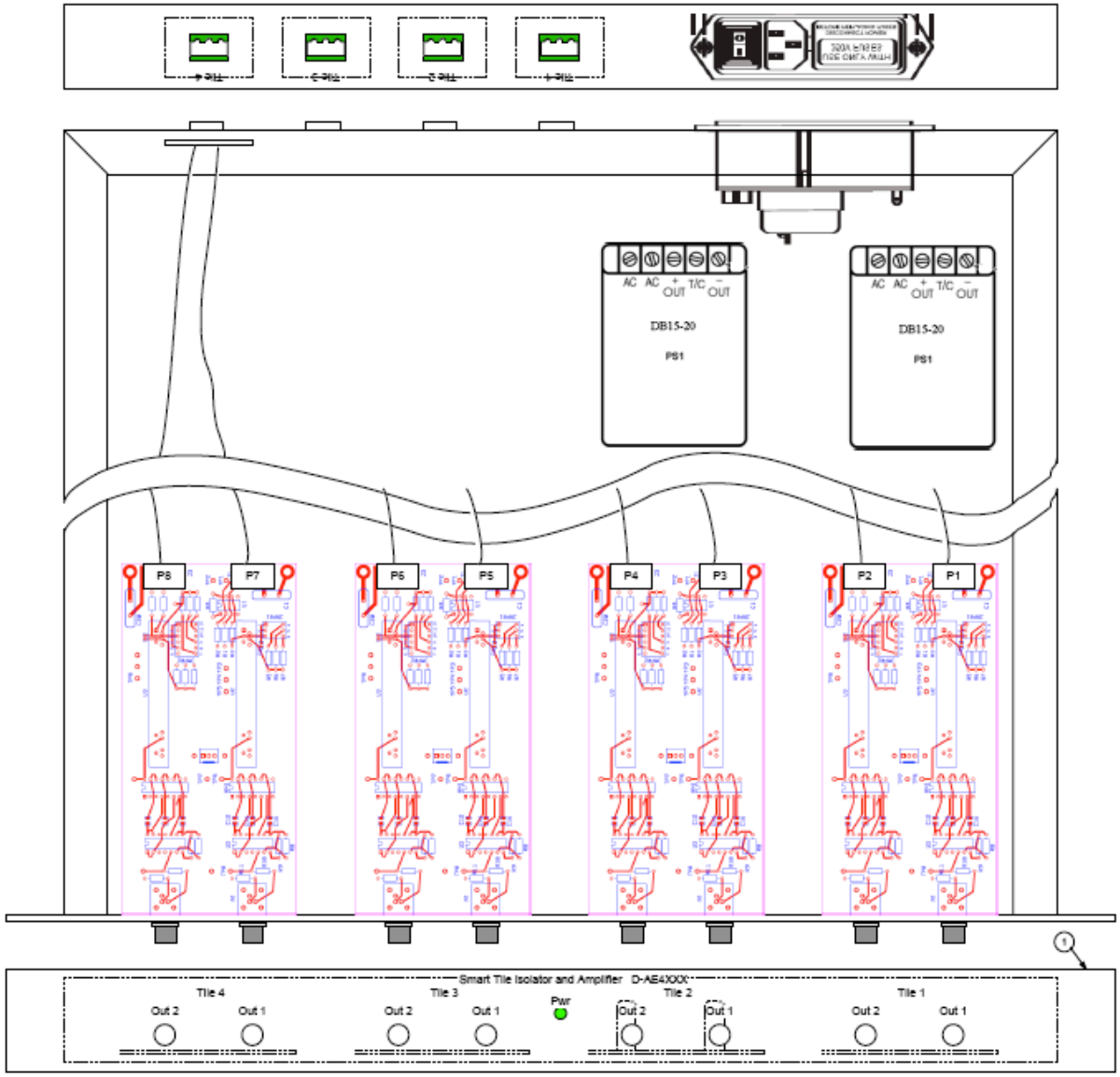
Solution

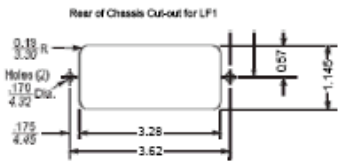
- Use AD-215 isolation amplifier for heavy lifting.
- 8 pole low-pass filter for anti-aliasing.
- 4 inputs and 8 outputs per single chassis to save space.

Design by E. Lawson and R. Marsala (I)



Design by E. Lawson and R. Marsala (II)





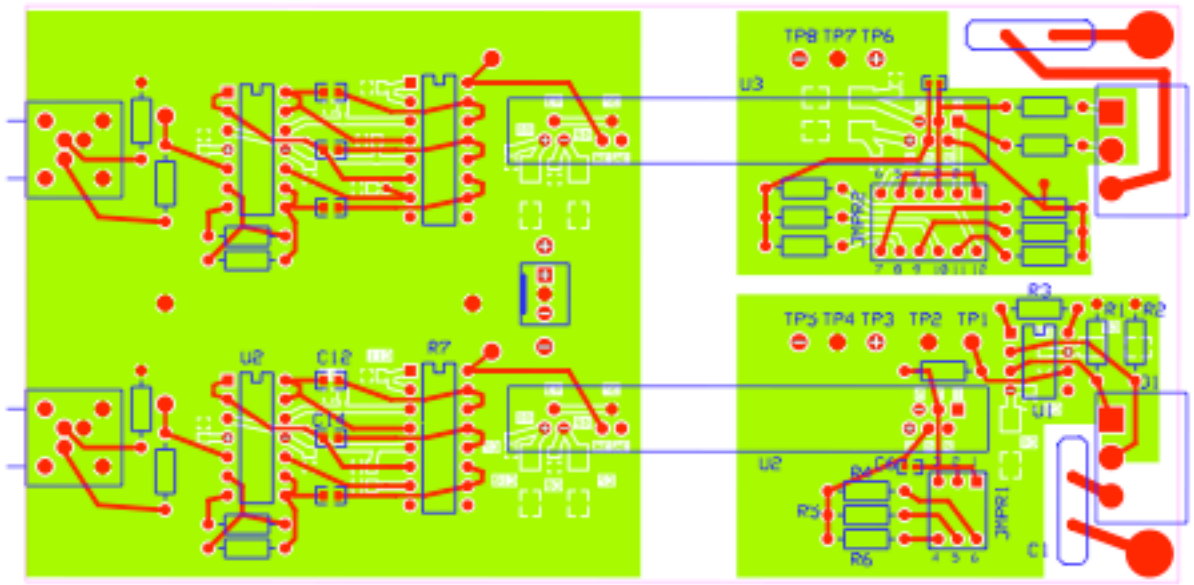
Design by E. Lawson and R. Marsala (III)

- 4 inputs, 8 outputs per chassis
- Estimated Initial Cost, including engineering: $14k unloaded, $24k loaded.
- Estimated Subsequent cost: $5 unloaded, $8k loaded.

4 per Chassis

Gozouta #2

Gozouta #1



Gozinta #1

Gozinta #2

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Start!

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In-Vessel Wiring Scheme

- Tile package has 2 stainless leads, which transition to copper twisted pair for the main in-vessel runs.
- Insulate the leads with glass tubing.
- For splicing stainless to copper twisted pair:
  - Hypodermic needle spot-welded wire (1/2 way up needle).
  - Hypodermic needle crimped to copper (1/2 way up needle).
- Route long twisted-pair copper leads to feedthrough on lower dome port.
- Feedthroughs on order, arriving soon.

Location of electronics, feedthrough.

- Option 1 Location For Electronics: LLD Racks (???)
  - Locations As Yet Undefined (am I wrong?).
  - Would need to find some new DAq (can we steal from LLD).
  - Overall, large level of uncertainty.
- Option 2 Location For Electronics: Concrete Floor Cat. 4 Racks
  - Rack-space is tight, buy can probably find room for a chassis in rack 418.
  - Suggest adding a short column of 32 cross-connects to this rack.
  - 5kHz DAq present in the operations digitizers.
  - Some fast Daq available in PC-5.
  - This is probably the best choice to start with, but may not be a solution if the system grows.
- Feedthrough recommendation is based in this choice.
  - A single 32-pin feedthrough on a lower-dome port (Bay I, Bay J,…)
  - Combine signals from 4 center-post rogowskis, and 4 tile current monitors.
  - Run a field cable to new cross-connects in rack 418.

To Do

Make Final Decisions (Feedthrough Committee?)

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Should be Simple to Calibrate

- Using water-jet cut shunts should ensure a high-degree of uniformity.
- However, method should be devised for in-situ calibration:
  - Use ~10A low voltage power supply.
  - Attach negative terminal to (grounded) NSTX vessel.
  - Attach positive terminal to insulated rod, with a copper “pad” on the end.
  - Drive ~10A through the sensor, and measure the voltage at the cross-connects.
  - Once setup, should take less than an hour.
- Need a procedure, and assessment of any safety issues.
- Need sensor leads in a measurable condition to do calibration (use the G. Gething breakout box).

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Summary

- We have a complete electrical and mechanical design for the sensor.
- Resistive shunt under the tile is designed to give reasonable signals without becoming a fuse.
- Minor modifications to the tiles, T-bars, and T-bar hardware are required.
- Thermal properties of the design appear to be reasonable.
- Electronics have a preliminary design and cost estimate.
- Feedthroughs have been ordered.
- Ready to proceed with final fabrication.