Controlling electrical properties of zinc oxide deposited by radio-frequency (RF) magnetron sputtering for use in thin film transistors

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Abstract

Initial characterization of sputtered zinc oxide films included resistivity measurements using both four point probe and transmission line method measurements, but it was found that the sputtered films were too resistive for the measurement tools. After post-deposition annealing at 300C and 400C, the resistivities were measured to be on the order of $10^3\Omega$-cm. However, even highly resistive films could be incorporated into working transistors, so the effect of different sputtering conditions on the films could still be characterized by transistor device characterization. Zinc oxide thin-film transistors (TFTs) were fabricated with a p-Si gate and aluminum source/drain contacts, and produced on/off currents on the order of 10^7. While the effect of specific sputtering parameters on the zinc oxide TFT properties were not able to be evaluated, it was demonstrated that the sputtering deposition produced conductive films that could be used to make working transistors. Fine tuning the zinc oxide TFTs electrical properties by adjusting more sputtering parameters is the anticipated next step.

1 Introduction

Zinc oxide is an oxide semiconductor with several desirable properties that make it a promising material for many electrical applications, such as electronic displays and surface acoustic wave (SAW) devices [1]. Zinc oxide can be deposited at relatively low temperatures, making it a viable semiconductor for use in thin film transitors with flexible plastic substrates. Further, its transparency and high electron mobility renders it a superior semiconductor to the existing industrial material, amorphous silicon.

Since zinc oxide films can be deposited via various methods such as thermal atomic layer deposition (ALD), pulsed laser deposition (PLD), and chemical vapor deposition (CVD), it is important to explore the parameters of each to determine the right processes for any given device application. Radio-frequency (RF) magnetron sputtering is one such method, especially scalable and thus effective for large area applications [2]. It is a plasma process in which the positive ions

in an Ar plasma are accelerated to hit a target (of ZnO, for example) with enough force to eject atoms from that target. Those molecules then travel to the counter-electrode where they condense onto the substrate. The addition of a strong magnetic field near the target confines the electrons to the area near the target so they won't interfere with the deposited film. It also allows the plasma to be made at low pressures, which will also reduce the inclusion of background gas into the film. The properties of the deposited zinc oxide films can be adjusted by the sputtering conditions, including the gas pressure, gas content (Ar/O_2), and temperature [3]. Zinc oxide is intrinsically an n-type semiconductor; the reason for this is contested, as some believe its n-type property is due to the oxygen vacancies (missing atoms at regular lattice positions) and zinc intersitials (extra atoms in the interstices of the lattice), while others believe it is due to impurities introduced during growth, namely, hydrogen [2]. Assuming the former hypothesis, increasing the oxygen content in the sputtering chamber would create less conductive films.

Ultimately, the goal is to find a set of sputtering conditions that can be used to deposit films of zinc oxide that can be incorporated into transistors with certain desired characteristics. Gaining control of the electrical properties of sputtered zinc oxide would greatly motivate its use in semiconductor devices. This study involved several phases, including semiconductor deposition, film resistivity measurements, transistor development, and transistor characterization, all of which will be discussed in greater detail below.

2 Methods and Results

2.1 Material Deposition

For the initial characterization, zinc oxide was sputtered onto 1"x3", 1.2 mm thick glass slides under different conditions, including various O_2 flow rates and deposition temperatures [4]. All of the sputtering recipes specified 3 millitorr gas pressure with no N_2, and 10 sccm Ar gas and produced films with a thickness of 100 nm. The glass slides were cleaned with acetone, isopropanol, deionized water, and then blow dried. A micro glass cover slide (22x22 mm) was used to shade part of the glass substrate to create a step with which the thickness of the zinc oxide was measured using a surface profiler [5]. An example of a single surface profiler measurement is shown below, demonstrating a measured height of 93 nm of one of the films. Some particles on the surface and unevenness of the glass and zinc oxide surface are shown as well.

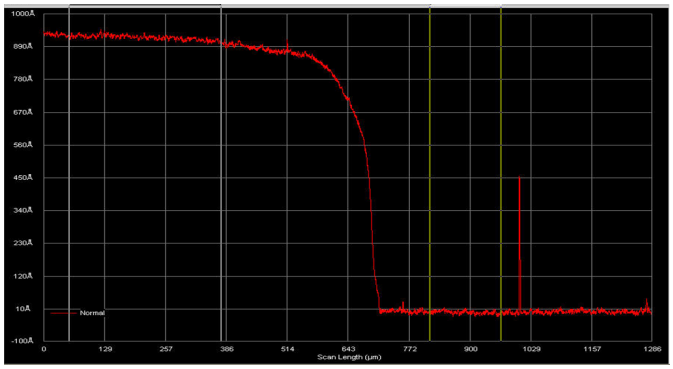


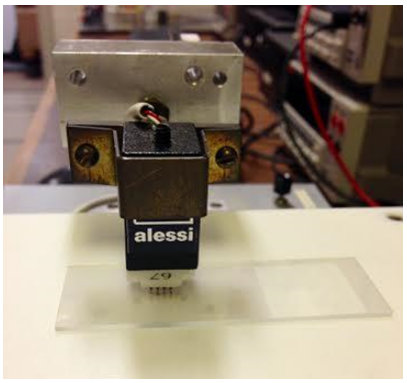
Figure 1: Surface profiler measurement of zinc oxide film thickness of 93 nm. The step is created by shading a part of the glass substrate with a micro glass cover slide.

2.2 Film Resistivity Measurements

Two methods of measuring ZnO resistivity were employed - the four-point probe and transmission line methods. Both methods require the measurement of sheet resistance and thickness to calculate the bulk resistivity as $\rho = R_s \times t$.

In the four-point probe method, the sheet resistance is measured as $R_s = \pi/ln(2) \times (V/I) \times k$, where k is a geometric correction factor that depends on the ratio of the dimensions of the sample to the spacing of the probes. The correction factors for these rectangular samples were determined via a formula and correction graphs [6]. The four-point probe measurement set up is shown in Figure 2. However, this tool could not measure the high resistivity of the sputtered zinc oxide films, as the readings were near the noise level of the probes, as shown in Figure 3(a)(b). To perform a check on the technique itself, thermal ALD zinc oxide samples (100 nm ZnO on Si) were measured using the four-point probe method, and the resistivity was measurable and corroborated by previous measurements, as seen in Figure 3(c).

(a)



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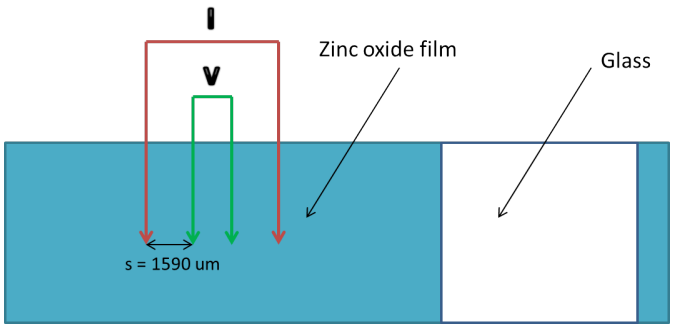


Figure 2: (a) Four point probe on ZnO deposited on glass (b) Diagram of placing and spacing of probes (1590 um) on glass.

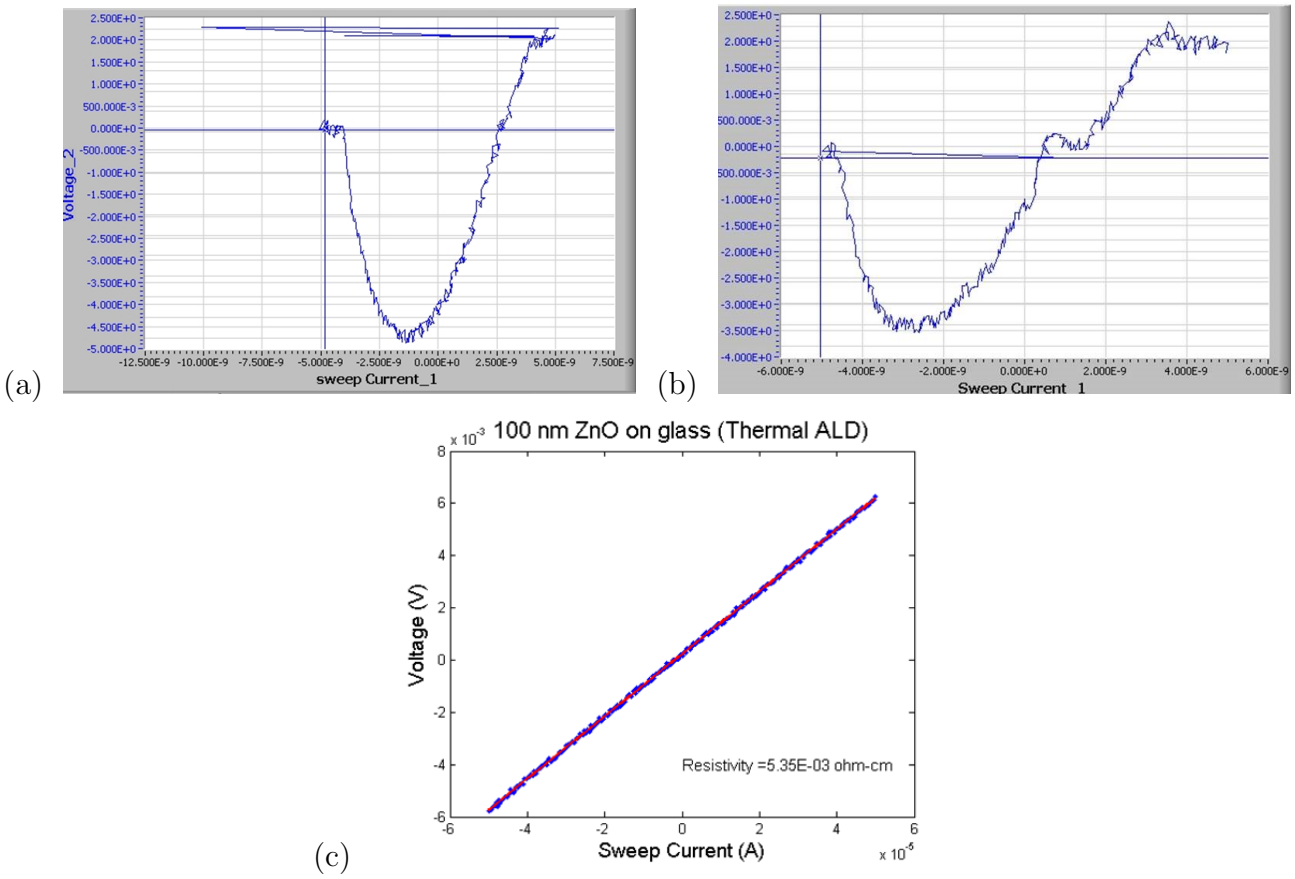
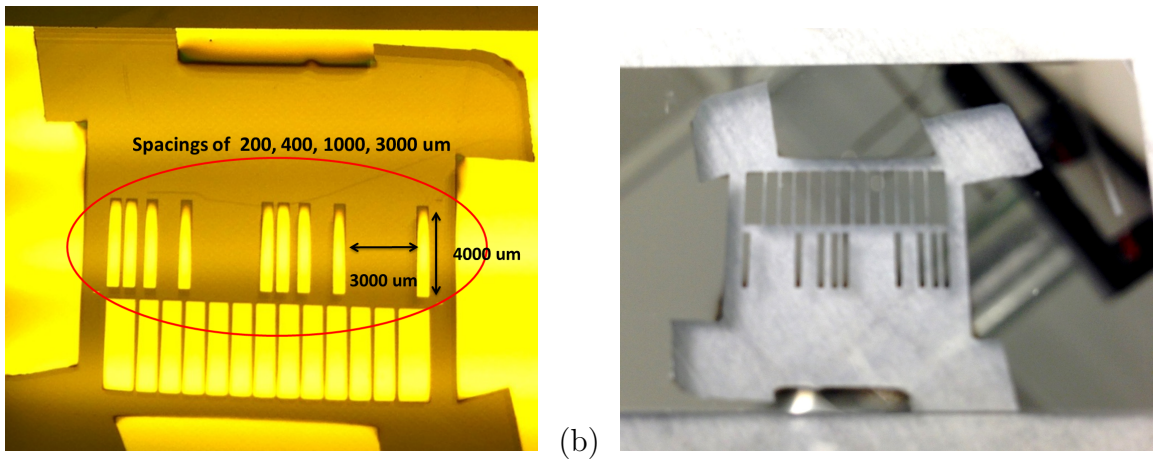


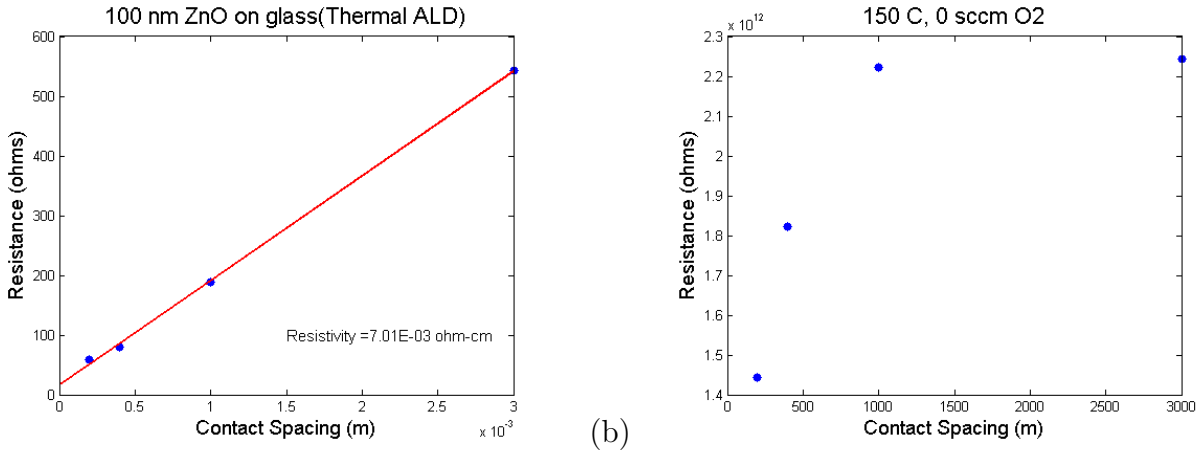
Figure 3: (a) Current-voltage (IV) curve for four point probe measurement of zinc oxide deposited on glass in 0 O2 and at 300C. Cannot determine sheet resistance from the nonlinear curve. (b) IV curve for no contact four point probe measurement, demonstrating the noise level of the instrument (sweeping current from -5e-9 to +5e-9 A results in voltage drops on the order of 1 V). (c) IV curve for thermal ALD ZnO samples with a calculated $\rho = 5 \times 10^{-3}\Omega$-cm.

The transmission line method (TLM) uses different spacings of metal contacts to interpolate the sheet resistance. The resistance between contacts vs. channel length curve is commonly used to determine metal-semiconductor contact resistance via the intercept, but the sheet resistance can also be extracted from the slope [7]. Specifically, the sheet resistance is calculated as the $R_s = slope \times z$, where z is the channel width. Using a shadow mask with channel lengths of 200, 400, 1000, and 3000 um and channel widths of 4000 um, aluminum was sputter-deposited on the zinc oxide (see Figure 4). These contact pads were probed consecutively and the resistance measurements were used to find the film's resistivity. However, the resistance vs. spacings curves for the sputtered zinc oxide films were not linear as they need to be for this measurement method. To test the tools, thermal ALD zinc oxide films were tested with the TLM method, and the results are shown in Figure 5(a). TLM measurements for the sputtered zinc oxide films are shown in Figure 5(b). The nonlinear curve of the sputtered films imply that their resistivities were too high to be measured, especially across the largest spacings.



(a) (b)

Figure 4: (a) Shadow mask for TLM measurements used to deposit 100 nm of aluminum on zinc oxide film on glass (b)100 nm Al deposited on ZnO on glass



(a) (b)

Figure 5: Resistance vs. Contact Spacing of (a) thermal ALD prepared zinc oxide films to calculate resistivity and (b) sputtered zinc oxide films (150C, no O_2 added to Ar sputtering gas).

Both measurement techniques, while shown to give reasonable, measurable results for more conductive samples, were not sufficient to detect the electrical conductance of the sputtered zinc oxide films on glass. Sputtering parameters, including O_2 flow rate, deposition temperature, and substrate-target distance were all adjusted to attempt to achieve measurable films, but no effects were visible. To ensure the target in the sputterer was zinc oxide, an x-ray photoelectron spectroscopy measurement was also done, which verified the composition of the film to be indeed zinc oxide.

2.3 Post-deposition annealing

In order to reduce the resistivity of the films enough so that they could be measured with the four-point probe, post-deposition annealing was attempted at different temperatures for different

lengths of time. The samples were annealed on a hot plate in the atmosphere at both 300C and 400C. After each 15 minute period, the samples would be measured with the four point probe, then placed back on the hot plate to start the next 15 minute anneal. The annealing tests were done on samples deposited without oxygen and at 300C – the four-point probe results of these samples before annealing are shown in section 2.2. After 60 minutes of annealing (4 successive anneal steps) at 300C, the measurement reached an order of magnitude above the noise level; at 15 minutes at 400C, the resistivity also reached an order of magnitude above the noise level. The four-point probe measurements for all of the aforementioned situations are shown below in Figure 6.

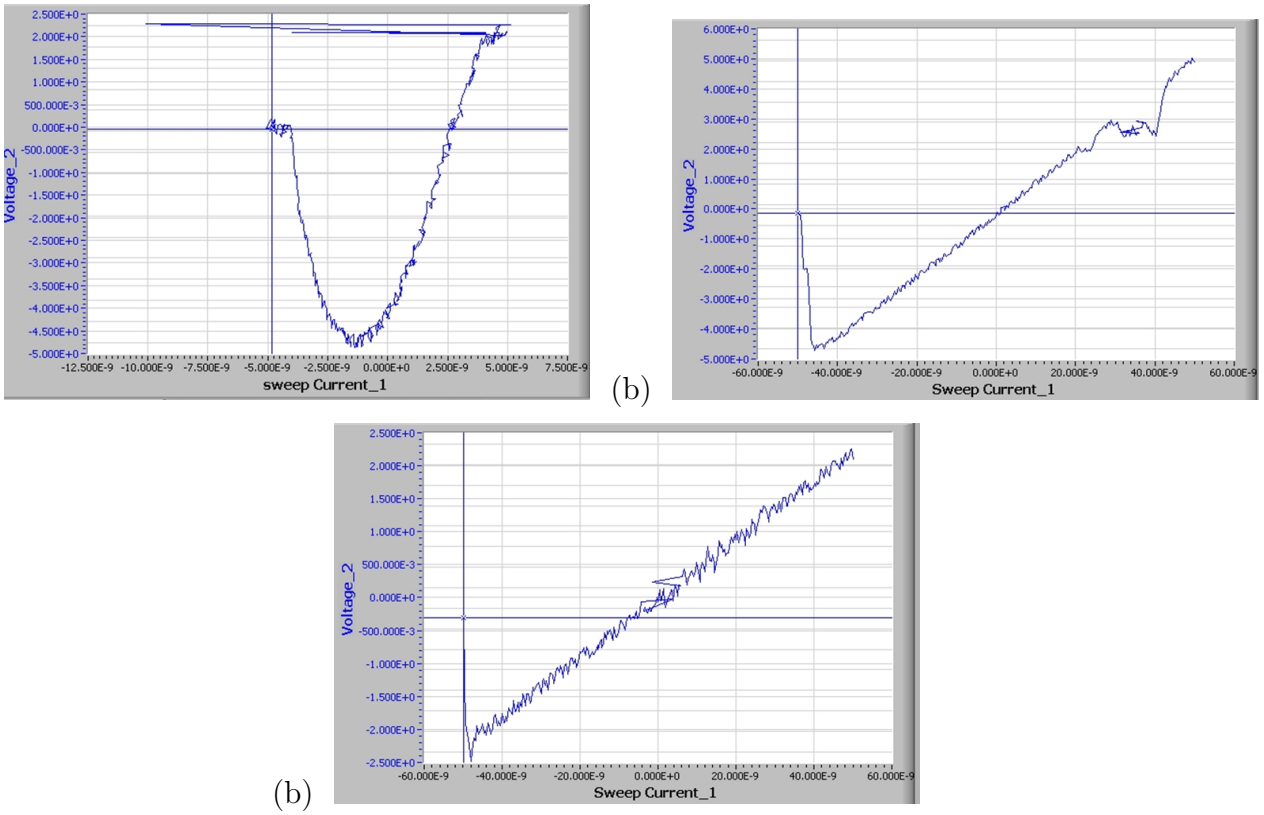


Figure 6: (a) Before annealing – notice the current is swept from -5e-9 to +5e-9 A. (b) After annealing at 300C for 60 min – notice the current is swept from -5e-8 to 5e-8 A. (c) After annealing at 400C for 15 min – again, notice the current is swept from -5e-8 to 5e-8 A.

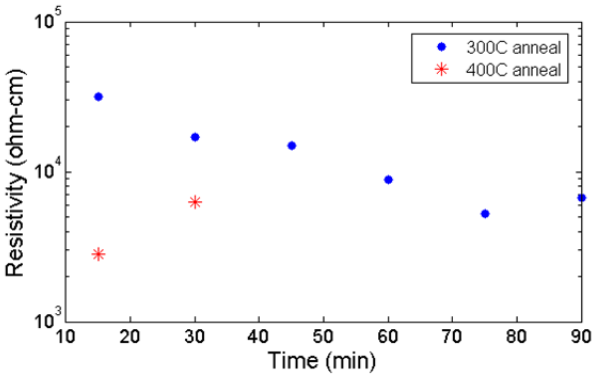


Figure 7: Zinc oxide resistivities after annealing at different temperatures and times. The lowest resistivity achieved was 2.7e3 Ω-cm, whereas the noise level of the probes (and previous, non-annealed samples) were on the order of 10^4.

The results of all annealing tests are shown above, demonstrating that annealing the zinc oxide samples helps us get more conductive, measurable films. However, it should also be noted that 400C was too high of a temperature beyond 15 minutes of annealing, as it caused the glass and film to crack after 30 minutes of annealing.

2.4 Transistor fabrication

Although the above methods of characterizing the electrical properties of the sputtered zinc oxide films were inadequate for the high level of resistivity of the samples unless they were annealed, the films could still be tested for use in thin film transistors (TFTs). While the transistor fabrication process is more involved and lengthy than simply depositing on glass slides, it allows us to characterize these films in a more applicable way. The hope was that the zinc oxide on glass slides would provide enough information about the effect of sputtering conditions on the electrical properties of sputtered zinc oxide (and their viability in TFTs) without requiring a more extensive process of transistor fabrication. However, since the above resistivity measurements failed, zinc oxide transistors were fabricated and measured. The process is described below and the transistor design is shown in Figure 8.

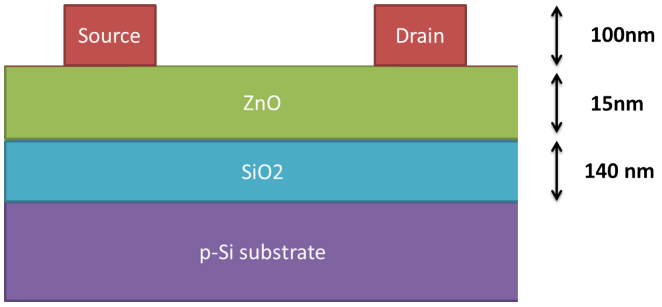
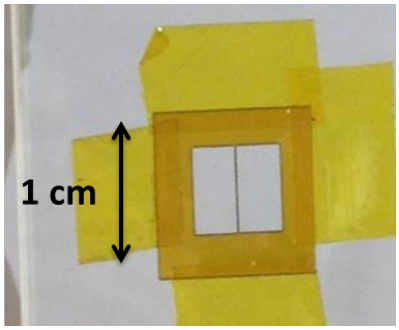


Figure 8: Schematic of the transistor design with a p+ Si gate and Al source and drain contacts.

Thermal oxide was first grown on silicon wafers. These oxidized wafers were cleaned with

acetone, IPA, and DI water before zinc oxide sputtering. 15 nm of zinc oxide was sputtered without oxygen at various substrate temperatures. During the first run, the sputtered film was immediately cleaned with acetone, which caused spotting on the sample, which could have been related to poor interface adhesion between the SiO2 and ZnO. In any case, the next processes did not include this post-sputtering cleaning step. Instead, source-drain lithography was immediately performed. Kapton shadow masks for the source and drain (Fig. 9(a)) were also tried, but as the channel lengths from the shadow masks could only be reduced to 125 um, lithography became a better option. See the appendix for information on making the shadow masks. The source-drain lithography masks included channel lengths ranging from 20 to 30 um (Fig. 9(b)).

(a) 

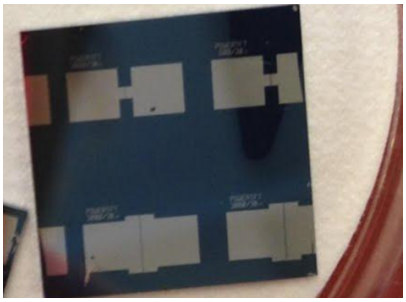
(b) 

Figure 9: (a) Source-drain shadow mask made by laser cutting Kapton. Channel length of 125 um was the smallest achieved resolution. (b) 30 um and 20 um channels on finished transistors using photolithography.

Photolithography processing included the following steps. The samples were first baked at 95C for 3 minutes. Hexamethyldisilazane (HMDS) was spin coated onto the sample in order to prime the sample for photoresist. HMDS serves as an adhesion promoter for the photoresist. The photoresist AZ5214 was then spin coated onto the sample at 4000 rpm [8]. The sample was then soft baked at 95C for 45 s. Then, using a mask aligner and a previously made source-drain mask, the samples were exposed for 30 s [9]. The sample was then baked at 100C for 1 min 15 s, before it was flood exposed for 60 s with no mask. Finally, it was developed in AZ300MIF for 1 minute and then rinsed with DI water and blow dried.

Almost immediately after the lithography steps, 100 nm aluminum was deposited on top via sputtering [10]. Liftoff of all of the metal except the source and drain requires about 5 minutes of sonication in acetone, then a rinse in IPA and DI water. The microscope image of the channel of some processed devices are shown below.

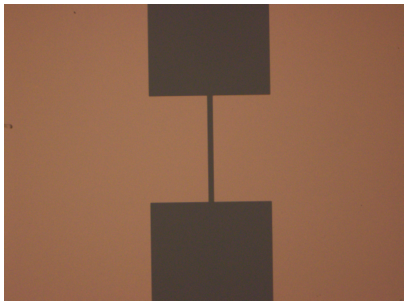
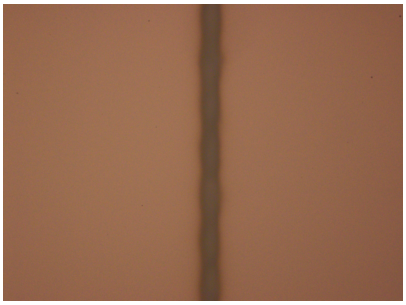
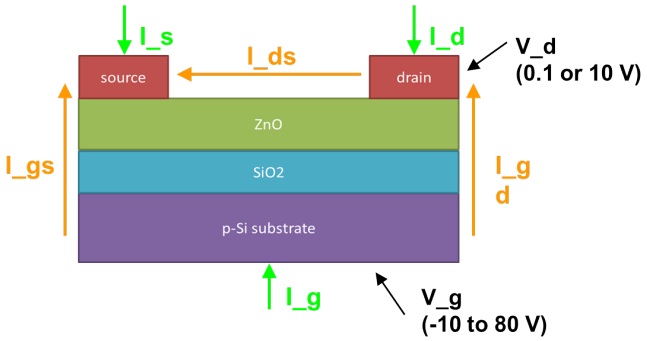
(a)  (b) 

Figure 10: (a) 30 um channel made with lithography (b) 125 um channel made with shadow mask

2.5 Transistor characterization

The devices were tested using a probe station and a semiconductor parameter analyzer. The set up is shown below in Figure 11. A drain voltage bias of 0.1 and 10 V were applied to all devices and the gate voltage was swept from -10 to 80 V in order to turn on many of the transistors. In order to calculate the current flowing from source to drain (I_{ds}) from the measured currents, a couple of assumptions were made. First, $I_g = I_{gs} + I_{gd}$ and $I_{ds} = I_d + I_{gd}$. Assuming $V_{gd} \sim V_{gs}$, then $I_{gd} \sim I_{gs}$, and we calculate from the first two equations that $I_{ds} = I_d + I_g/2$.

(a) 

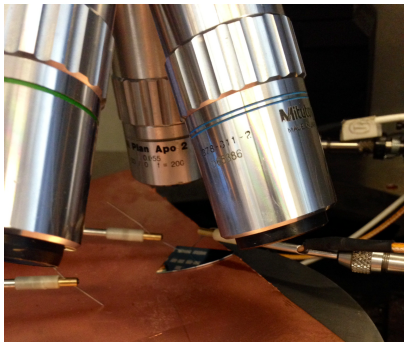
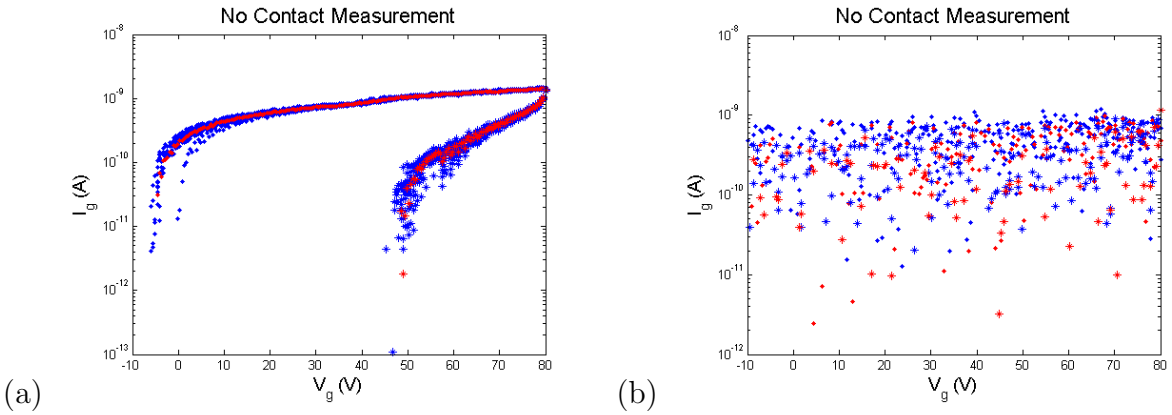
(b) 

Figure 11: (a) TFT measurement set up. The green arrows represent where the probes contact and measure the device. The orange arrows demonstrate what currents need to be extracted from the raw measurements. (b) Probe station set up with the copper printed circuit board to create better electrical contact to the gate.

To create better electrical contact to the silicon gate, the backs of the samples were scratched with a diamond scriber to remove any native oxide. One challenge was the high gate current measured, and the hysteresis observed when sweeping up and then down (see Figure 12a). To attempt to reduce the gate current, a copper PCB board (copper on the top, insulator on the bottom) was placed between the probe chuck and sample, to again, get better electrical contact (see Figure 11b). However, this still did not eliminate the high gate current measured, though it did eliminate the previous hysteresis (see Figure 12b). This "no contact" gate current was used to calibrate the subsequent measurements of I_{ds}.



(a) (b)

Figure 12: Measured gate current from no probe contact to source/drain (but gate contact to chuck), (a) without copper PCB board and (b) with copper PCB board. The upper curve is sweeping up, and the lower is sweeping down.

Transistors made with zinc oxide deposited at different temperatures (21C, 100C, 200C, 300C) and no O2 were tested and shown below.

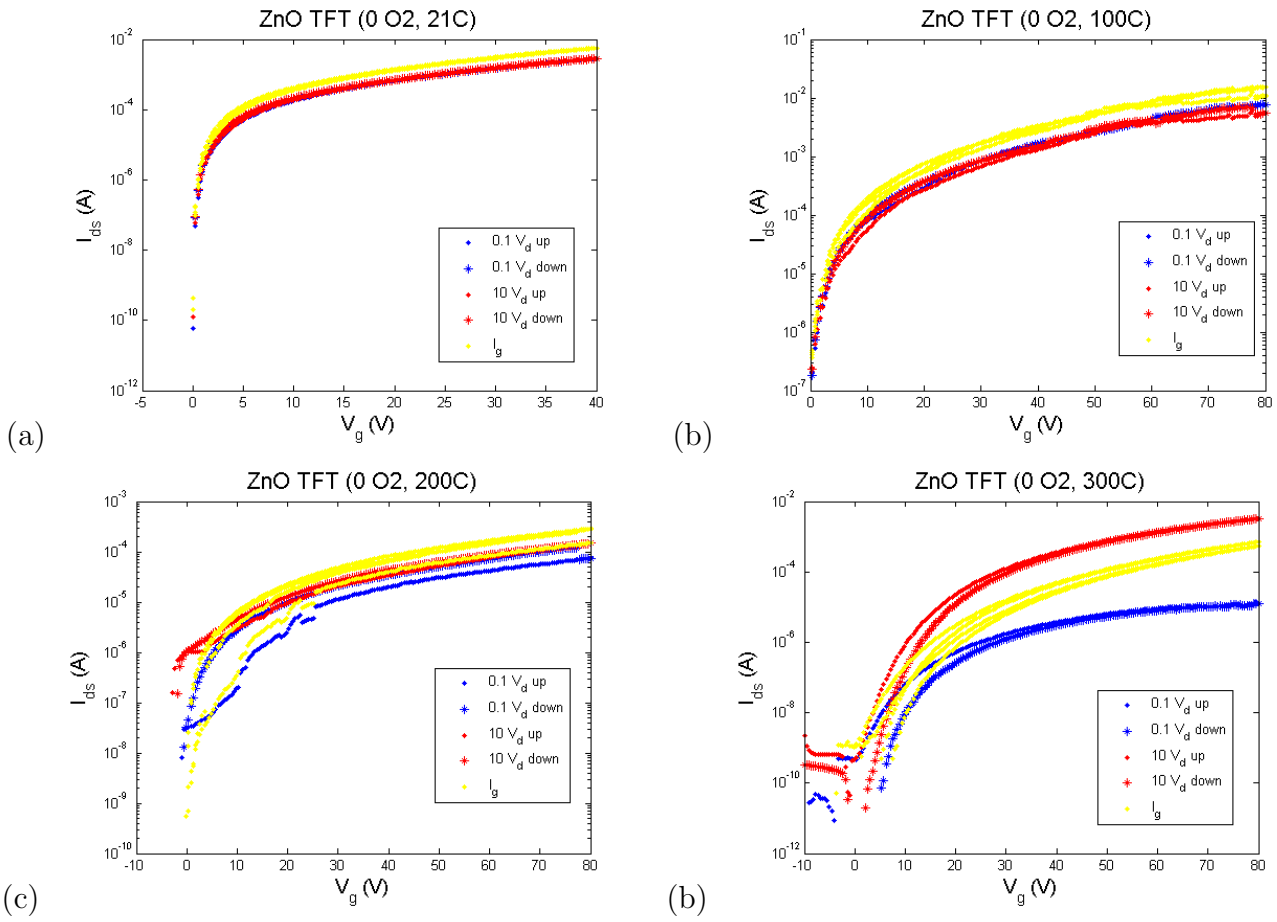


Figure 13: Drain-source current vs. Gate voltage for zinc oxide TFTs made from different sputtering conditions. Blue curves are drain voltage bias of 0.1 V; red are drain voltage bias of 10 V; yellow are gate current curves.

The transistors made at 300C exhibit an on/off current ratio of about 10^7 and a threshold voltage of about 10 V. Even when varying the drain bias from 10 to 40 V, saturation was not observed.

3 Discussion and Conclusion

This project's goal was to determine sputtering recipes to deposit films of zinc oxide for use in thin-film transistors and to observe how different sputtering parameters affect the electronic properties of zinc oxide.

Conductive zinc oxide films were sputtered in pure argon environments and when post-deposition annealed; however, the resistance of the films was so high that they could not be measured with a four-point probe or TLM. Therefore, since the films on glass were not measurable, another step was taken to fabricate TFTs out of the sputtered zinc oxide and measured their transfer characteristics, which allowed me to evaluate the films' resistances. While there are still unsolved problems in the measurement of these TFTs (namely, the high gate current), it is still clear that the devices

function (on-off current ratio of about 10^7) with the films sputtered at various temperatures. In the future, I would like to continue fabricating TFTs with different zinc oxide sputtering conditions, including different temperatures, O_2 flow rate, RF power, and post-deposition annealing temperatures/times. After getting reasonable transistor gate currents and better contacts to the gate, I would analyze the transfer characteristics of those samples, including on/off ratios, threshold voltages, and subthreshold slopes. Completion of all of this would provide a set of sputtering recipes with parameters that can be altered to control the electrical properties of zinc oxide for use in different devices. Control of the electrical properties of sputtered zinc oxide would help expand its use in the variety of potential applications.

4 Acknowledgements

I would like to thank the Program in Plasma Science and Technology Program and Professor Sigurd Wagner for making this valuable internship possible. Thank you also to Joseph Palmer, Conrad Silvestre, and David Radcliffe for training me to use the tools essential for my research. Thank you to the entire Large-Area Electronics group for productive conversations, presentations, and weekly advice. And finally, thank you to Prof. Wagner and Levent Aygun for their mentorship, guidance, and encouragement throughout the project.

References

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[7] http://www.che.ufl.edu/ren/course/4404L/MOS/TLM.pdf

[8] http://www.princeton.edu/prism/mnfl/the-tool-list/headway-spinners/

[9] http://www.princeton.edu/prism/mnfl/the-tool-list/karl-suss-ma6/

[10] http://www.princeton.edu/prism/mnfl/the-tool-list/angstrom-sputterer/

5 Appendix

5.1 Kapton Shadow Masks

Shadow masks were made by laser-cutting openings of the desired dimensions in 50 um thick foils of Kapton. To achieve the 125 um channel lengths of the kapton shadow masks, the power, pulses per inch (PPI), and speed were adjusted. The kapton was attached to a piece of acrylic by placing some droplets of water in between the surfaces. The laser cutter thus cut through the kapton on top of the acrylic. There are two sets of laser cutter parameters for the 125 um channels that I found to work the best. First, 40% power, 100% speed, 500 PPI, with a material thickness of 0.005", repeated 3 times. The other used 5% power, 20% speed, 500 PPI, thickness of 0.005", repeated 8 times. Both create a relatively strong channel that can be fixed to a glass slide or Si wafer by using kapton tape. However, before using them on the glass or Si, the charring needs to be cleaned off by using a cotton swab and IPA.

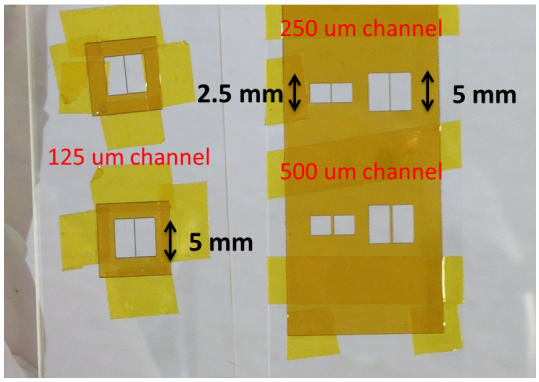

Figure 14: Shadow masks for source and drain attached with kapton tape to glass slides. Includes 125, 250, and 500 um long channels with channel widths of 2.5 and 5 mm.