Photosensitive a-Si Thin-Film Transistors

Michaela L. Hennebury

Advisor: Prof. James C. Sturm

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Background and Motivation

Since the first effective chimeric antigen receptor (CAR) T cells were built in a lab in 2002 [1], CAR T cell gene therapy has developed into a promising treatment for types of leukemia and lymphomas and has the potential to treat other cancers in the future. Unfortunately, many of the current manufacturing procedures for CAR T cells involve multi-step manual processes that result in significant cell loss. A deterministic lateral displacement (DLD) microfluidic device, however, can speed up the blood cell separation process and eliminate hands-on steps, making it a potentially superior alternative to current cell harvesting techniques [2]. Despite its benefits, DLD cell harvesting is not without fault. The device can sometimes become blocked and disrupt the process, and there is currently no practical way to tell when this happens. The long-term goal of this project is to develop a way to detect blocked areas in a DLD device so that the problem can be fixed, or so the device can be used in an alternative way to achieve cell separation.

One possible way to determine whether part of a DLD device is blocked is to use photosensitive thin-film transistors (TFTs). These transistors would have variable I-V characteristics depending on the intensity of white light they were exposed to. If they were situated on the side of the DLD device opposite from a light source, the TFTs behavior would change based on how much light passed through the device, thus indicating whether there was a blocked area.

The goal of this summer's work was to modify an existing recipe for amorphous silicon TFTs for use with available processing tools and to then evaluate their photosensitivity. Amorphous silicon (a-Si) was chosen as the active material for these TFTs because of its known

optoelectronic properties. Previous studies have demonstrated a-Si to be very photosensitive [3] and it has been used extensively in photodetectors and solar cells.

Process Overview

The procedure for a-Si TFT fabrication is based on those found in Warren Rieutort-Louis's and Tiffany Moy's theses [4, 5] with some key differences. For nitride and a-Si deposition, the Oxford PlasmaPro 100 ICP-CVD is used instead of the 4-chamber PECVD. This process also does not include doped a-Si and therefore uses a thinner intrinsic a-Si active layer. The following outlines the key steps in the process.

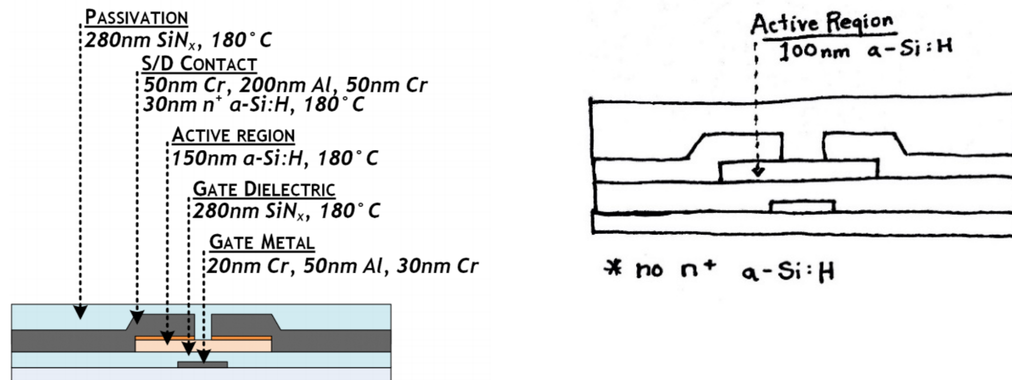

Figure 1: The structure of previously fabricated a-Si TFTs (left) [4] and the proposed structure for this project. This project uses a 100nm rather than a 150nm a-Si layer and does not have doped a-Si. For the purposes of this project, it was not necessary to use Al in the gate and source/drain metal, so only Cr was used for these layers.

First, a glass substrate is cleaned with a standard glass cleaning procedure. In order to accommodate the deposition and etching tools, ~1cm corners of the glass must be removed so that it can be mounted onto a 100mm wafer. This is done by scoring the glass with a glass cutter and snapping off the corners. The substrate should first be coated in photoresist so that glass dust does not stick to or damage the surface. The photoresist is removed afterwards with acetone before beginning TFT fabrication.

Before depositing the gate metal, the sample is covered with 150nm nitride as a passivation layer. Then, 50nm chromium is deposited with thermal evaporation and etched to form a gate pattern. The 280nm SiN_x gate dielectric and 100nm a-Si active layer are deposited one after another in the ICP-CVD. The active layer and gate via patterns are created using dry

etching. Finally, the source/drain contacts are patterned before metal deposition (100nm Cr), and the unwanted metal is removed through liftoff by sonicating the sample in acetone. At this stage in the process, the TFTs can be tested. For this project, the processing was finished after this initial test. For improved stability, a top passivation layer of SiN_x would be deposited and patterned and the completed sample would be annealed in vacuum at 200°C for 1 hour.

Plasma-Enhanced Chemical Vapor Deposition (PECVD)

As mentioned previously, the procedure used for this project differs from previous work in that it uses a different tool for gate dielectric (SiN_x) and active layer (a-Si) deposition. The ICP-CVD uses an inductively coupled plasma for deposition rather than a capacitively coupled plasma (used in the 4-chamber PECVD). Since a different tool was being used, a new a-Si recipe was developed, and experiments were conducted to determine the new deposition rates. A comparison of the two recipes is shown in the following table.

Table 1: PECVD a-Si recipes

	4-chamber PECVD	*Oxford ICP-CVD*
Pressure	500 mTorr	18 mTorr
Power	4W (RF)	500W (ICP)
Temperature	200C	250C
Gases/Flow Rate	SiH_4 (16 sccm) H_2 (200 sccm)	4% SiH_4/Ar (400 sccm) H_2 (100 sccm)
Deposition Rate	2.5 nm/min	1.3 nm/min

Because of the different chamber designs and methods of generating plasmas, it is difficult to compare the pressure and power for these two recipes. The temperature of 250C was chosen for the new recipe because higher temperature depositions generally result in better quality films. Unhydrogenated a-Si has a high defect density which is undesirable for TFT fabrication, so hydrogen is added to both recipes to lower the density of dangling bonds. The ratio of H_2 to SiH_4 is lower in the new recipe due to tool constraints.

To determine the deposition rate of the ICP-CVD a-Si recipe, a sample was covered with 120nm of SiO_2 followed by 2 hours of a-Si deposition. The thickness measurement of the a-Si

layer on the SiO_2 was performed with the reflectometer, and the results are shown in the following figure.

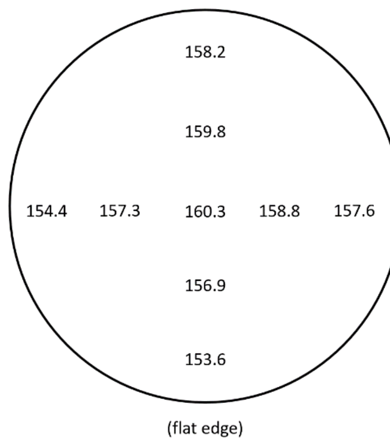

Figure 2: Thickness of a-Si after 120 minutes of deposition on different positions of a 4-inch wafer. Results are shown in nanometers.

The deposition rate was found to be roughly 1.3nm/min with 4% nonuniformity. A deposition time of 75 minutes was chosen to achieve a 100nm active layer in the TFTs.

Plasma Etching

Both the a-Si and the SiNx were etched with a plasma "dry" etch process. The a-Si was etched in the SAMCO 800 with a technique known as the Bosch process. This allows for high-aspect ratio silicon etching with alternating isotropic etch and passivation steps. The recipe used in this procedure uses an SF_6 plasma to etch the a-Si, followed by a C_4F_8 plasma that creates a Teflon-like passivation layer on the exposed surface. Each plasma lasts for one second and the sequence is repeated until the unwanted material is completely removed. To determine the etch rate of this process, a wafer was coated with 150nm of a-Si and patterned with photoresist. The sample was then subjected to 20 cycles of the Bosch process. The photoresist was then removed, and the step height was measured with a profilometer.

The SiN_x is etched in the PlasmaTherm 720. This uses a CF_4/O_2 plasma to remove unwanted material. An experiment similar to the one described above was conducted to determine this process's etch rate. For this test, the SiN_x was etched for 2 minutes. The results for both of these experiments are shown.

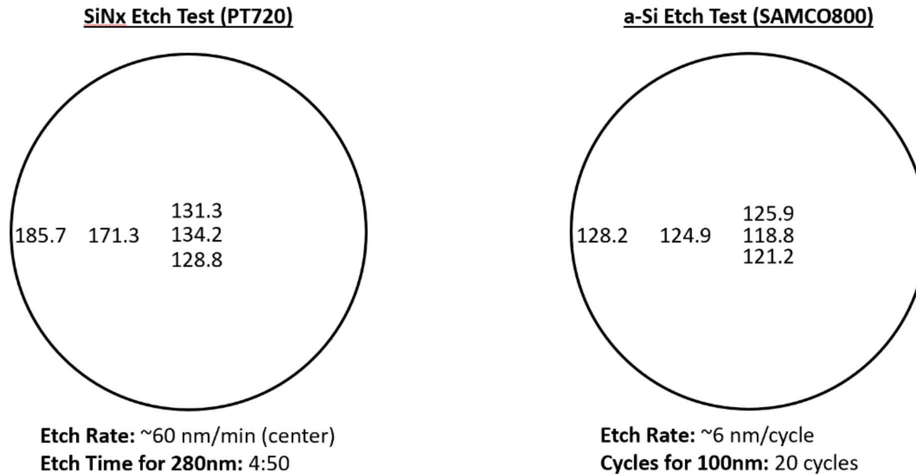

Figure 3: Plasma etch test results for SiN_x and a-Si. All measurements are shown in nanometers.

Based on these results, an etch time of 4 minutes and 50 seconds was chosen for 280nm of SiN_x in the fabrication process. This etch process was quite non-uniform, so extra time was added to guarantee that the gate metal was accessible in all areas of the sample. 20 cycles of the Bosch process were used to etch the 100nm a-Si active layer.

Results

The following is an example I-V curve for one of the TFTs fabricated for this project.

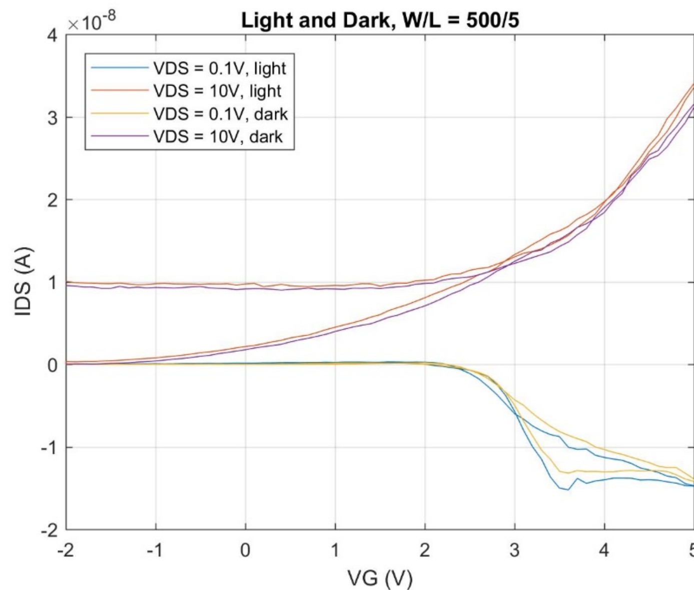

Figure 4: An I-V curve for an a-Si TFT with W/L of 500um/5um in the dark and in the light. The TFT was tested in both the linear (V_{DS} = 0.1V) and saturation (V_{DS} = 10V) regimes.

These TFTs demonstrated significantly lower currents than other a-Si TFTs fabricated in the past. For instance, at a V_{GS} of 5V and V_{DS} of 10V, these devices have an I_{DS} on the order of nanoamperes while previous work on TFTs of similar dimensions resulted in currents on the order of microamperes [4]. One possible reason for this is the lack of an n+ doped a-Si layer, which cannot be deposited with the available equipment. Another factor to consider is that these TFTs are not passivated with a top layer of SiN_x. Amorphous silicon degrades over time without passivation, negatively affecting the devices. Given that these measurements were conducted several weeks after device fabrication, it is reasonable to assume that this would undermine their performance. Yet another explanation is the lower H_2:SiH_4 ratio in the new a-Si PECVD recipe due to the ICP-CVD having a maximum of 100sccm of H_2. With a lower concentration of hydrogen during deposition, it is likely that the resulting a-Si has more dangling bonds.

A notable feature of these measurements is the negative drain-source current at low V_{DS}, which indicates gate leakage. This is also supported by the high gate current measurements when the gate voltage exceeded 2V, shown below. Additionally, most of the devices on the sample could not be measured due to high gate currents (greater than 10uA) that would break the transistors.

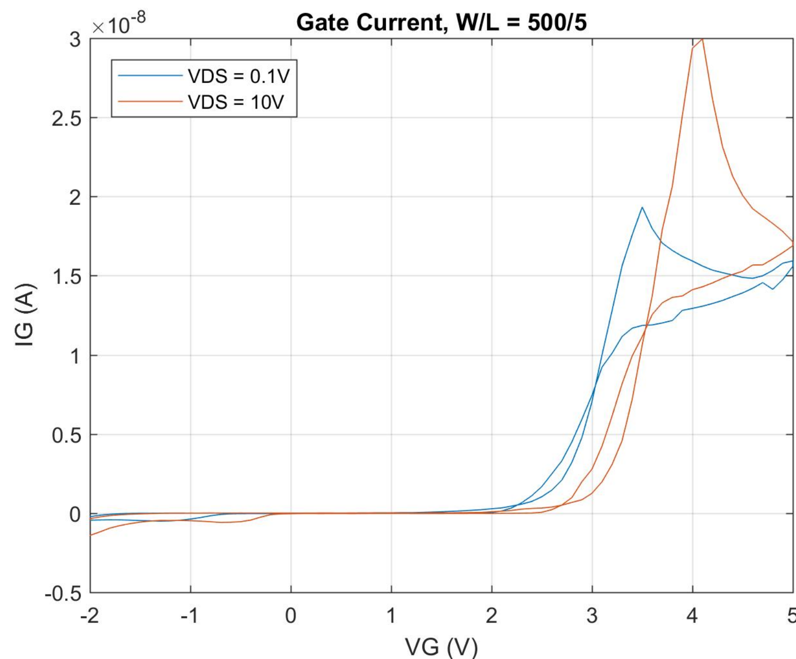

Figure 5: Gate currents for an a-Si TFT with W/L of 500um/5um in linear and saturation regimes. The gate current is on the same order of magnitude as the device source-drain current.

This gate leakage problem is most likely related to the insulating SiN_x layer. To confirm this, capacitors were fabricated with the same deposition and etch procedures as the TFTs and were found to be shorted. There are a few possible explanations for this issue, including poor insulator quality, roughness of gate metal, and charge introduced by plasma etching. Additional experiments need to be conducted to locate and remedy the cause of the problem. The TFTs also did not demonstrate significantly different behavior in light and dark environments. Once the fabrication process is improved to produce consistent, functioning TFTs, their photosensitivity can be explored further.

Conclusion and Future Work

The project for this summer was centered on developing a recipe for a-Si TFTs. While progress have been made, there is still much work to be done. This work confirmed that the available tools can be used to create TFTs and outlined an initial fabrication procedure, including deposition and etch times. The next step is to significantly improve the device performance, namely by finding and fixing the cause of the high gate currents. This will be done by creating SiN_x capacitors on both silicon and glass (with chromium metal) substrates with and without the plasma etch step. By analyzing the I-V behavior of these capacitors, the source of the gate leakage should become clear. After this is resolved, experiments will be conducted to determine the optoelectronic properties of the TFTs with the end goal of developing a system to detect blockages in DLD devices.

References

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